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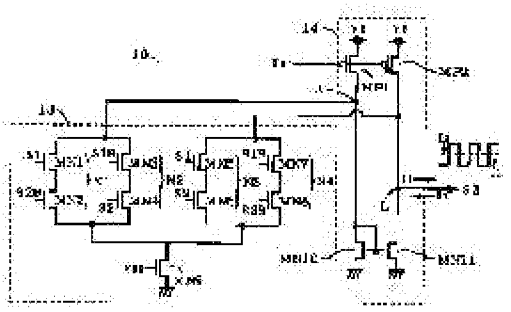
(54) NINETY-DEGREE PHASE SHIFTER

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a 90° phase shifter which has a uniform input load and prevents phase offsetting.
SOLUTION: Transistors(TR) MP1 and MP2 supply currents I0 to nodes K and L respectively, and TRs MN10 and MN11 draw mutually equal currents out of the nodes K and L respectively. A parallel connection of series-connection body N1 and N2 draws a current I1 out of the node K, only when exclusive OR of clocks S1 and S2 is 'H'. A parallel connection of series-connection bodies N3 and N3, meanwhile draws a current I1 out of the node L, only when the exclusive OR of the clocks S1 and S2 is 'L'. Once the current I1 is drawn out of the node K, a current I1 flows out of the node L and when the current I1 is drawn out of the node L, a current I1 flows in the node L. The series-connection bodies N1 to N3 receive the clocks S1 and S2 and their inverted signals S1B and S2B at one of the gates of the TRs MN1 to MN8, so that the input loads become uniform.



* NOTICES *

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2.**** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1]The 1st current control circuit that has a current mirror circuit characterized by comprising the following, The 1st portion that draws out the 2nd current from said 1st node only when exclusive OR of the 1st and 2nd signals takes the 1st logic, The 2nd current control circuit that has the 2nd portion that draws out said 2nd current from said 2nd node only when exclusive OR of said 1st and 2nd signals takes said 1st logic and the 2nd different logic, It is a phase shifter about 90 degrees provided with the 1st low pass filter connected to said 2nd node, and a delay part which delays said 1st signal by a delaying amount controlled by output potential of said 1st low pass filter, and outputs said 2nd signal.
The 1st and 2nd nodes.
The 1st current source that supplies the 1st current to said 1st node.
The 2nd current source that supplies said 1st current to said 2nd node.
The 1st course that draws out current from said 1st node, and the 2nd course that draws out current from said 2nd node.

[Claim 2]It is a phase shifter the about 90 degrees according to claim 1 which has the 1st capacitor and the 1st end connected to said 2nd end of said resistance characterized by comprising the following, and the 2nd end connected to said 2nd end of said 1st capacitor, and is provided with the 2nd capacitor with larger capacity value than said 1st capacitor.
The 1st end by which said 1st low pass filter was connected to said 2nd node.
Resistance which has the 2nd end from which said output potential of said 1st low pass filter is obtained.
The 1st end connected to said 1st end of said resistance.
The 2nd end.

[Claim 3]Said 1st low pass filter is a phase shifter the about 90 degrees according to claim 2 further provided with a current supply source mechanism which makes an initial state of said 2nd capacitor a charging state.
[Claim 4]It is a phase shifter the about 90 degrees according to claim 1 further provided with an offset cancel circuit characterized by comprising the following.
A plus input end which makes an input signal said output potential of said 1st low pass filter.
A negative input terminal.
A differential amplifier containing an outgoing end which outputs a control signal which controls said delaying amount with said output potential of said 1st low pass filter.

A dummy part which makes connection equivalent to said 1st course of said 1st current source and said current mirror circuit, is connected to said negative input terminal of said differential amplifier, and contains a dummy node corresponding to said 1st node.

[Claim 5]Said offset cancel circuit is a phase shifter the about 90 degrees according to claim 4 which is inserted between said 1st low pass filter and said plus input end of said differential amplifier, and has further the 2nd low pass filter with a bigger damping time constant than said 1st low pass filter.
[Claim 6]Have the 2nd transistor characterized by comprising the following, and said 2nd current source A drain, The 1st transistor that has sauce and a backgate which were connected common to said 2nd node, and a gate where said 1st bias is impressed, It is a phase shifter the about 90 degrees according to claim 1 provided with the 2nd transistor that has said sauce of said 2nd transistor of said 1st current source, connected sauce, a drain connected to said drain of said 1st transistor of said 2nd current source, and a gate where said 2nd bias is impressed.
Said 1st current source is a drain.
Sauce connected common to said 1st node, and a backgate.
The 1st transistor that has a gate where the 1st bias is impressed.
Sauce, a drain connected to said drain of said 1st transistor, and a gate where the 2nd bias is impressed.

[Claim 7]It is a phase shifter the about 90 degrees according to claim 6 further provided with the 3rd transistor characterized by comprising the following.
A drain with which said 1st current source was connected to said drain of said 1st transistor of said 1st current source.
Sauce connected in common with said drain of said 2nd transistor of said 1st current source, and a backgate.
A drain which was further provided with the 3rd transistor that has a gate where the 3rd bias is impressed and with which said 2nd current source was connected to said drain of said 1st transistor of said 2nd current source.
Sauce and a backgate which were connected in common with said drain of said 2nd transistor of said 2nd current source, and a gate where said 3rd bias is impressed.

[Claim 8]It has the 1st and 2nd series connection bodies characterized by comprising the following that are a phase shifter and were mutually connected in parallel between said 1st current source and said output node about 90 degrees as for said 1st switch, Have said 2nd switch and the 1st and 2nd series connection bodies mutually connected in parallel between said 2nd current source and said output node said 1st series connection body of said 1st switch, The 1st transistor that flows when said 1st signal takes said 1st logic, Comprise a series connection with the 2nd transistor that flows when said 2nd signal takes said 2nd logic, and said 2nd series connection body of said 1st switch, The 1st transistor that flows when said 1st signal takes said 2nd logic, Comprise a series connection with the 2nd transistor that flows when said 2nd signal takes said 1st logic, and said 1st series connection body of said 2nd switch, The 1st transistor that flows when said 1st signal takes said 1st logic, The 1st transistor that comprises a series connection with the 2nd transistor that flows when said 2nd signal takes said 1st logic, and flows through said 2nd series connection body of said 2nd switch when said 1st signal takes said 2nd logic, It is a phase shifter about 90 degrees which comprises a series connection with the 2nd

transistor that flows when said 2nd signal takes said 2nd logic.
The 1st current source.
The 2nd current source.
An output node.
The 1st switch that flows only when it is provided between said 1st current source and said output node and exclusive OR of the 1st and 2nd signals takes the 1st logic, The 2nd switch that flows only when it is provided between said 2nd current source and said output node and exclusive OR of said 1st and 2nd signals takes said 1st logic and the 2nd different logic, A delay part which delays said 1st signal by low pass filter connected to said output node, and a delaying amount controlled by output potential of said low pass filter, and outputs said 2nd signal.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This inventions are insides, such as a digital disposal circuit, for example, the receiving circuit of a radio signal, and a processing circuit of a computer, and relate to the delay circuit (in this application, this is called a phase shifter about 90 degrees) outputted so that the inputted signal may be made into 1/4 of the cycle, and a phase and it may become 90-degree delay.
[0002]
[Description of the Prior Art]Drawing 14 is a timing chart which shows a relation with the clock S1 which changes to the same timing as the cycle of transition of the data S6, and transition of the data S6, and a phase. In the digital disposal circuit which receives such the data S6 and the clock S1, The way things stand, when the clock S1 changes, the data S6 has changed, and the data S6 cannot be latched appropriately to latch the data S6 using the standup of the clock S1, or transition of falling. Then, it will be necessary to shift the phase of the clock S1 to the data S6.
[0003]Drawing 15 is the timing chart which made the phase timing to which the clock S1 changes to the timing to which the data S6 changes, and was able to shift it 90 degrees. By doing in this way, the standup of the clock S1 or the timing of falling serves as a center (center of the timing of transition that the data S6 adjoins) of the eye pattern of the data S6, and the latch of the data S6 using transition of the clock S1 becomes the most certain.
[0004]Drawing 16 is a circuit diagram showing the outline of the input interface of the chip 91 which inputs the data S6 and the clock S1. Respectively the data S6 and the clock S1 spread the transmission lines 110a and 110b of the chip 91 exterior, result in the pad electrodes 111a and 111b of chip 91 inside, and are buffered by the buffers 112a and 112b, respectively. The 90-degree phase shift of about 90 degrees of the clocks S1 is carried out by the phase shifter 200 after that, and the clock S2 is generated.
[0005]The data S6 buffered by any data-input-terminals D of the latch circuitry 113a and 113b is given, and the clock S2 is given to which clocked into end T. However, the latch circuitry 113a latches the data S6 at the time of the standup of the clock S2, and the latch circuitry 113b latches the data S6 at the time of falling of the clock S2.
[0006]Drawing 17 is a circuit diagram which illustrates about 90 degrees of composition of the phase shifter 200. The phase shifter 200 is provided with about 90 degrees of the PLL (Phase-LockedLoop) circuits 120 and the delay stages 5. PLL circuit 120 is provided with VCO circuit 122, the phase comparator 121, and the low pass filter 2. Signal S9 by which the reference signal

S7 and the phase were locked is generated by this PLL circuit 120. In this case, delay control signal S4 obtained from the low pass filter 2 is adopted as the delay control of the delay stage 5, and the clock S1 buffered by the buffer 112b is in 90 degrees in the delay stage 5, and turns into the output clock S2.
[0007]the time of PLL circuit 120 locking about 90 degrees by the phase shifter 200 -- delay in VCO circuit 122 -- the cycle of the reference signal S7 -- so that it may become half (a phase is used and it is 180 degrees) exactly, Delay control signal S4 from the number and the low pass filter 2 of the buffer 4 of VCO circuit 122 inside is set up. And the output of the couple from the buffer 4 of a final stage carries out a positive/negative inversion, and is connected to the input of the couple of the buffer 4 of the stage at first. By this, when the reference signal S7 is given, VCO circuit 122 will be stabilized and will be oscillated, and signal S9 locked with the same cycle as the reference signal S7 and the phase will be obtained.
[0008]Then, the signal shifted only one fourth of cycles to the clock S1 is generable as the clock S2 by adopting the clock S1 as the reference signal S7, and having the buffer 4 of the half of the number of the internal buffers 4 with which the delay stage 5 constitutes VCO circuit 122. That is, as long as PLL circuit 120 locks, the delay produced in the delay stage 5 is not dependent on a process or other conditions, is made into a phase, and is held at 90 degrees.
[0009]
[Problem(s) to be Solved by the Invention]However, generally there was a problem of the increase of hard quantity and the increase of power consumption which are produced from being a problem of destabilization and VCO being required in a PLL circuit.
[0010]It is going to solve this problem and the art of performing a 90-degree phase shift without using PLL circuit 120 is also proposed. Drawing 18 is a circuit diagram which illustrates about 90 degrees used about 90 degrees in drawing 16 replacing by the phase shifter 200 of composition of the phase shifter 201. The composition of the phase shifter 201 removes about 90 degrees of VCO circuits 122 under composition of the phase shifter 200, and has about 90 degrees of composition which transposed about 90 degrees of phase comparators 121 to the phase detector circuit 100. That is, the phase shifter 201 constitutes about 90 degrees of DLL (Delay-Locked Loop) circuits.
[0011]Drawing 19 is a circuit diagram which illustrates about 90 degrees of composition of the phase detector circuit 100. The phase detector circuit 100 is provided with about 90 degrees of EXOR circuits 10a and the charge pump circuits 11.The clock S1 and the exclusive OR of S2 which were acquired by EXOR circuit 10a are changed into UP / DOWN signal S3 which takes the mode of current in the charge pump circuit 11. In order to supply UP / DOWN signal S3, the current source as which a current amount is determined by a bias signal, respectively is provided in the charge pump circuit 11.
[0012]UP / DOWN signal S3 is given to the low pass filter 2, the current amount integrates with it, it is changed into a direct-current voltage signal, and delay control signal S4 to the delay stage 5 is obtained. Feedback is hung by this delay control signal S4 to the delay for obtaining the clock S2 from the clock S1.
[0013]However, it receives that the clock S1 passes a transfer gate or a NOT circuit, and reaches the charge pump circuit 11 in EXOR circuit 10a, Since the clock S2 is only applied to the gate which manages ON/OFF of a transfer gate, the clock S1 and S2 will receive different input load in EXOR circuit 10a. For this reason, there was a problem that the clock S2 will balance with the phase [degrees / 90] shifted to the clock S1 (below, this gap is called phase offset).
[0014]In order to solve this, adopting EXOR circuit 10b constituted like drawing 20 instead of

EXOR circuit 10a is also considered. Although the clock S1 and the input load to S2 become equal with this composition, since the compound gate is used, many transistor counts will be needed, and the problem that circuit structure becomes large will arise.
[0015]It was made in order that this invention might solve the above-mentioned problem, and it aims at obtaining about 90 degrees with easy circuitry of phase shifters. It aims also at obtaining the phase shifter which equalized load about the signal which is two by which a phase should be locked. It aims also at the improvement of phase offset.
[0016]
[Means for Solving the Problem]What starts claim 1 among this invention The 1st and 2nd nodes, The 1st current source that supplies the 1st current to said 1st node, and the 2nd current source that supplies said 1st current to said 2nd node, The 1st current control circuit that has a current mirror circuit including the 1st course that draws out current from said 1st node, and the 2nd course that draws out current from said 2nd node, The 1st portion that draws out the 2nd current from said 1st node only when exclusive OR of the 1st and 2nd signals takes the 1st logic, The 2nd current control circuit that has the 2nd portion that draws out said 2nd current from said 2nd node only when exclusive OR of said 1st and 2nd signals takes said 1st logic and the 2nd different logic, About 90 degrees provided with the 1st low pass filter connected to said 2nd node and a delay part which delays said 1st signal by a delaying amount controlled by output potential of said 1st low pass filter, and outputs said 2nd signal are a phase shifter.
[0017]The 1st end according to claim 1 by which about 90 degrees of things which start claim 2 among this invention are phase shifters, and said 1st low pass filter was connected to said 2nd node, Resistance which has the 2nd end from which said output potential of said 1st low pass filter is obtained, It has the 1st capacitor that has the 1st end connected to said 1st end of said resistance, and the 2nd end, the 1st end connected to said 2nd end of said resistance, and the 2nd end connected to said 2nd end of said 1st capacitor, and has the 2nd capacitor with larger capacity value than said 1st capacitor.
[0018]The about 90 degrees according to claim 2 of things which start claim 3 among this invention are phase shifters, and said 1st low pass filter is further provided with a current supply source mechanism which makes an initial state of said 2nd capacitor a charging state.
[0019]The plus input end according to claim 1 which about 90 degrees of things which start claim 4 among this invention are phase shifters, and makes an input signal said output potential of said 1st low pass filter, A differential amplifier containing a negative input terminal and an outgoing end which outputs a control signal which controls said delaying amount with said output potential of said 1st low pass filter, Connection equivalent to said 1st course of said 1st current source and said current mirror circuit is made, and it is connected to said negative input terminal of said differential amplifier, and has further an offset cancel circuit which has a dummy part containing a dummy node corresponding to said 1st node.
[0020]The about 90 degrees according to claim 4, it is a phase shifter which starts claim 5 among this invention, and said offset cancel circuit, It is inserted between said 1st low pass filter and said plus input end of said differential amplifier, and has further the 2nd low pass filter with a bigger damping time constant than said 1st low pass filter.
[0021]The about 90 degrees according to claim 1 of things which start claim 6 among this invention are phase shifters, and said 1st current source A drain, The 1st transistor that has sauce and a backgate which were connected common to said 1st node, and a gate where the 1st bias is impressed, Sauce and a drain connected to said drain of said 1st transistor, Have the 2nd transistor that has a gate where the 2nd bias is impressed, and said 2nd current source A drain,

The 1st transistor that has sauce and a backgate which were connected common to said 2nd node, and a gate where said 1st bias is impressed, It has the 2nd transistor that has said sauce of said 2nd transistor of said 1st current source, connected sauce, a drain connected to said drain of said 1st transistor of said 2nd current source, and a gate where said 2nd bias is impressed.
[0022]The drain according to claim 6 with which about 90 degrees of things which start claim 7 among this invention are phase shifters, and said 1st current source was connected to said drain of said 1st transistor of said 1st current source, Sauce and a backgate which were connected in common with said drain of said 2nd transistor of said 1st current source, A drain which was further provided with the 3rd transistor that has a gate where the 3rd bias is impressed and with which said 2nd current source was connected to said drain of said 1st transistor of said 2nd current source, It has further the 3rd transistor that has sauce and a backgate which were connected in common with said drain of said 2nd transistor of said 2nd current source, and a gate where said 3rd bias is impressed.
[0023]What starts claim 8 among this invention The 1st current source and the 2nd current source, The 1st switch that flows only when it is provided between an output node, and said 1st current source and said output node and exclusive OR of the 1st and 2nd signals takes the 1st logic, The 2nd switch that flows only when it is provided between said 2nd current source and said output node and exclusive OR of said 1st and 2nd signals takes said 1st logic and the 2nd different logic, About 90 degrees provided with a low pass filter connected to said output node and a delay part which delays said 1st signal by a delaying amount controlled by output potential of said low pass filter, and outputs said 2nd signal are a phase shifter, Said 1st switch has the 1st and 2nd series connection bodies mutually connected in parallel between said 1st current source and said output node, Have said 2nd switch and the 1st and 2nd series connection bodies mutually connected in parallel between said 2nd current source and said output node said 1st series connection body of said 1st switch, A series connection of the 1st transistor that flows when said 1st signal takes said 1st logic, and the 2nd transistor that flows when said 2nd signal takes said 2nd logic is comprised, The 1st transistor through which said 2nd series connection body of said 1st switch flows when said 1st signal takes said 2nd logic, Comprise a series connection with the 2nd transistor that flows when said 2nd signal takes said 1st logic, and said 1st series connection body of said 2nd switch, The 1st transistor that flows when said 1st signal takes said 1st logic, Comprise a series connection with the 2nd transistor that flows when said 2nd signal takes said 1st logic, and said 2nd series connection body of said 2nd switch, About 90 degrees which comprises a series connection of the 1st transistor that flows when said 1st signal takes said 2nd logic, and the 2nd transistor that flows when said 2nd signal takes said 2nd logic are a phase shifter.
[0024]
[Embodiment of the Invention]Embodiment 1. drawing 1 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 1 of composition of the phase detector circuit 101.
[0025]The phase detector circuit 101 is provided with about 90 degrees of the EXOR sections 13 and the current control 14. The EXOR section 13 comprises the Nch transistors MN1-MN8 of the characteristic, and Nch transistor MN9 mutually. The current control 14 is mutually constituted from the Nch transistors MN10 and MN11 of the characteristic by Pch transistorMP1 of the characteristic, MP2, and each.
[0026]In the EXOR section 13, the drains of transistor MN5 and MN7 are connected in common

for the drains of transistor MN1 and MN3, respectively. The sauce of transistor MN3 and the drain of transistor MN4 are connected with the sauce of transistor MN1 for the drain of transistor MN2, respectively. The sauce of transistor MN7 and the drain of transistor MN8 are connected with the sauce of transistor MN5 for the drain of transistor MN6, respectively. And the sauce of transistor MN2, MN4, MN6, and MN8 is connected in common. the clock S1 -- the gate of transistor MN1 and MN5 -- give the inversion signal S1B to the gate of transistor MN3 and MN7, the clock S2 is given to the gate of transistor MN4 and MN6, and the inversion signal S2B is given to the gate of transistor MN2 and MN8, respectively. The drain of transistor MN9 is connected common to the sauce of transistor MN2, MN4, MN6, and MN8, and the sauce of transistor MN9 is grounded. Bias potential V_{BN} is impressed to the gate of transistor MN9.

[0027]In the current control 14, bias potential V_{BP} is given to the sauce of transistor MP1 and MP2 for power-supply-potential V_D in common at the gate, respectively. The sauce of transistor MN10 and MN11 is grounded in common. With the drain and gate of transistor MN10, the drain of transistor MP1 is connected to the drain of transistor MN1 and MN3 in common in the node K. With the drain of transistor MN11, the drain of transistor MP2 is connected to the drain of transistor MN5 and MN7 in common in the node L. UP / DOWN signal S3 is acquired by the node L as current which flows / flows out.

[0028]In the EXOR section 13, when the clock S1 and S2 take the same logical value, one of transistors turns off by the series connection body N1 which transistor MN1 and MN2 constitute. One of transistors turns off also by the series connection body N2 which transistor MN3 and MN4 constitute similarly. Therefore, the series connection body N1 and N2 turn off the branch by which multiple connection was carried out as a whole. On the other hand, in both the series connection bodies N3 that transistor MN5 and MN6 constitute, when the clock S1 and S2 are High(s), both transistor MN5 and MN6 turn on. In both the series connection bodies N4 that transistor MN7 and MN8 constitute, when the clock S1 and S2 are Low(s), both transistor MN5 and MN6 turn on. Therefore, the series connection body N3 and N4 turn on the branch by which multiple connection was carried out as a whole.

[0029]In taking the clock S1 and the logical value from which S2 differs, in the series connection body N3 and N4, one of transistors turns off and it turns off the series connection body N3 and the branch to which multiple connection of N4 was carried out as a whole. On the other hand, the series connection body N1 and either of N2 turn on.

[0030]As mentioned above, the series connection body N1 and the multiple connection of N2 flow, only when the clock S1 and the exclusive OR of S2 are "H", and the series connection body N3 and the multiple connection of N4 flow, only when the clock S1 and the exclusive OR of S2 are "L."

[0031]Drawing 2 is a circuit diagram showing about 90 degrees in case the clock S1 and S2 take the same logical value of equivalent circuits of the phase detector circuit 101. In a figure, the gate where the upward arrow was added shows that logic"H" is given (also setting on the following drawings the same). Bias potential V_{BP} was impressed equally to the gate of transistor MP1 and MP2, and since power-supply-potential V_D is impressed equally, the drain has required the voltage between sauce gates equal also to which transistor MP1 and MP2. both [for this reason,] transistor MP1 and MP2 -- although -- current I_0 is passed equally.

[0032]Transistor MN10 and MN11 constitute the current mirror circuit, and since the series connection body N1 and the branch to which multiple connection of N2 was carried out are moreover turned off as a whole, current equal to current I_0 which transistor MP1 passes flows into transistor MN10 and MN11. On the other hand, since transistor MN9 passes current I_1 based

on bias potential V_{BN}, current I_1 is drawn in the current control 14 as UP / DOWN signal S3 from the path connected to the low pass filter 2. Hereafter, current I_1 calls a down period the period drawn in the current control 14 in this way.

[0033]Drawing 3 is a circuit diagram showing about 90 degrees in the case of taking the clock S1 and the logical value from which S2 differs of equivalent circuits of the phase detector circuit 101. When the path which goes to transistor MN9 has arisen from the drain side of transistor MN10, transistor MP1 passes current I_0 and transistor MN9 is passing current I_1, Current (I_0-I_1) will flow into transistor MN10 and MN11. Since transistor MP2 passes current I_0, current I_1 flows out of the current control 14 into the low pass filter 2 as UP / DOWN signal S3. Hereafter, current I_1 calls a rise period the period which flows into the low pass filter 2 in this way.

[0034]Drawing 4 is the timing chart which also added the clock S1, S2 and contrast attachment, and delay control signal S4 for UP / DOWN signal S3 generated as mentioned above. However, the direction out of which it thinks on the basis of the current control 14, is considered as UP / DOWN signal S3, and current flows into the low pass filter 2 is made positive, and the direction which flows from the low pass filter 2 is made negative. About 90 degrees of this embodiment, since about 90 degrees shown in drawing 18 of phase detector circuits 101 can be replaced and used for the phase detector circuit 100, below, they are explained also with reference to drawing 18.

[0035]Considering the case where adjustment of a phase is started from the state where the delay value of the delay stage 5 is less than 90 degrees, as for about 90 degrees of UP / DOWN signals S3 from the phase detector circuit 101, the direction of a down period becomes longer than a rise period. Therefore, delay control signal S4 produced by integrating with UP / DOWN signal S3 in the low pass filter 2, and changing into the voltage of a direct current falls on the average, although there is some exception in a rise period. Therefore, the delay value of the delay stage 5 increases, and when it amounts to one fourth of cycles, about 90 degrees of the rise periods and down periods of UP / DOWN signal S3 of the phase detector circuit 101 become equal. That is, the phase of the clock S2 balances later than it of the clock S1 90 degrees.

[0036]When the delay value of the delay stage 5 starts adjustment of a phase from a bigger value than 90 degrees, as for UP / DOWN signal S3, the direction of a rise period becomes longer than a down period. Therefore, delay control signal S4 goes up on the average, although there is some exception in a down period, and a delay value causes the decreasing tendency. And the phase of the clock S2 balances later than it of the clock S1 90 degrees like the case of the point.

[0037]Drawing 5 is a circuit diagram which illustrates the composition of the delay stage 5. The delay stage 5 is provided with the delay control circuit 50 and the delay buffer part 51. The delay control circuit 50 is provided with Nch transistor MN12, MN13, Pch transistorMP7 and MP8, and the resistance R3. The sauce of transistor MN12 is grounded via the resistance R3, and the drain is connected common to the drain and gate of transistor MP7. Power-supply-potential V_D is given to the sauce of transistor MP7 and MP8 in common, and the drain of transistor MP8 is connected to the gate and drain of transistor MN13. The sauce of transistor MN13 is grounded.

[0038]Current is supplied to the potential side with the high delay buffer part 51 by the Pch transistor, The plurality of the inverter ("delay inverters" is called in this invention) with which current is drawn out has the composition connected in series with the Nch transistor from the low potential side, and the clock S1 which is the target of delay is given to the delay inverters of the stage at first. Since the transistor which specifies the current supplied to delay inverters constitutes the current mirror circuit with transistor MP8 or MN13, the delaying amount in each delay inverters is determined by the current which flows into transistor MN12. Since delay

control signal S4 is given to the gate of transistor MN12, as the delay stage 5 whole, the delaying amount of the delay stage 5 will be controlled by delay control signal S4. Of course, the current which flows into transistor MN12 can change the resistance of the resistance R3, and can also be adjusted.

[0039]Drawing 6 is a circuit diagram which illustrates the composition of the low pass filter 2. One end of capacitor CP0 is connected to the 1st end (end by the side of the left in the figure) of the resistance R1, one end of capacitor CP1 is connected to the 2nd end (end by the side of figure Nakamigi), respectively, and the other end of capacitor CP0 and CP1 is grounded in common. UP / DOWN signal S3 is given to the 1st end of the resistance R1. The capacity value of capacitor CP0 is set up very small as compared with the capacity value of capacitor CP1.

[0040]Since it is easy, if capacitor CP0 is disregarded and considered, the resistance R1 and capacitor CP1 will mainly be integrated with an inflow/outflow of current I_1 to the low pass filter 2 by UP / DOWN signal S3, it will be mostly changed into the voltage of a direct current, and will obtain delay control signal S4.

[0041]The function of capacitor CP0 makes small change of delay control signal S4 always according [current I_1] to the inflow/flowing out to the low pass filter 2. Speaking qualitatively, controlling the high frequency component (jitter) of current I_1 with the damping time constant determined by capacitor CP0 and the resistance R1, and controlling change of the voltage given to the gate of transistor MN12 of the delay control circuit 50. Since the capacity value of capacitor CP0 is dramatically small as compared with the capacity value of capacitor CP1, it hardly depends for the damping time constant in this case on the value of capacitor CP1. However, it is clear to operation of this embodiment that existence of capacitor CP0 is not indispensable.

[0042]The function to set the potential of capacitor CP1 as power-supply-potential V_D based on the reset signal S8 may be applied to the 2nd end of the resistance R1. If the protective diode D1 in preparation for the case where capacitor CP1 is specifically charged more than power-supply-potential V_D, and the switch SW switch on based on the reset signal S8 are formed in series between the potential point which gives power-supply-potential V_D, and the 2nd end of the resistance R1, the above-mentioned function is realizable. By adding this function, the reset signal S8 can be inputted by an initial state, capacitor CP1 can be charged, and current can be started to transistor MN12 from the maximum and the state where made it pass and the delay value of the delay stage 5 was always made into the minimum.

[0043]As mentioned above, in a phase shifter, since not PLL circuit 120 but DLL circuit 201 was adopted, when the frequency of the oscillating frequency of VCO circuit 122 and the clock S1 has a difference, about 90 degrees realized by this embodiment of things for which an error will be integrated are avoided. Since the clock S1 is only compared with the clock S2 produced by delaying this in DLL circuit 201, the addition of the above errors is not produced but there is an advantage of excelling in stability.

[0044]Control of the phase offset by the difference of input load which had been produced when EXOR circuit 10a of the former [about 90 degrees / section / 13 / of the phase detector circuit 101 / EXOR] adopted as a phase shifter was used about 90 more degrees, Being able to realize by a small transistor count as compared with EXOR circuit 10b by a compound gate, circuit structure does not increase. As compared with the charge pump circuit 11 which about 90 degrees of phase detector circuits 100 need, the circuit structure of the current control is small, or even if the current control 14 of the phase detector circuit 101 is large, there are few about 90 degrees of the differences. Phase offset can be controlled by composition produced by replacing

about 90 degrees which constitutes after all about 90 degrees which is a DLL circuit of phase shifters of phase detector circuits [about 90 degrees of] 100 in the phase detector circuit 101, without increasing circuit structure.
[0045]Drawing 7 is a timing chart which shows transition of the clock S2 when the period of "H" of the clock S1 is longer than the period of "L", and drawing 8 is a timing chart which shows transition of the clock S2 when the period of "H" of the clock S1 is shorter than the period of "L." a figure -- inside -- a period -- ** - ** -- respectively -- a clock -- S -- one -- S -- two -- (-- " -- H" -- " -- L -- " --) -- (-- " -- H" -- " -- H" --) -- (-- " -- L -- " -- " -- H" --) -- (-- " -- L -- " -- " -- L -- " --) -- a value -- taking -- a period -- being shown -- **** .
[0046]Since delay control signal S4 is controlled based on the clock S1 and the exclusive OR of S2, when the sum total of period ** and period ** and the sum total of period ** and period ** become equal, the clock S2 is locked to the clock S1. And since the clock S2 is in 90 degrees to transition of the clock S1, each of period ** and ** is made into a phase, a 90-degree period is maintained, the sum total of period ** and period ** is made into a phase, and a 180-degree period is maintained.
[0047]When the period of "H" of the clock S1 is longer than the period of "L", a falling edge is located in the timing that only delta 2 is late, from the center beta of the period of "L" at the timing that only the center alphadelta1 of the period of "H" of the clock S1 of the rising edge of the clock S2 is early, respectively. When the period of "H" of the clock S1 is shorter than the period of "L", As for the rising edge of the clock S2, only delta 3 is located in late timing from the center alpha of the period of "H" of the clock S1, and a falling edge is located in the timing that only delta 4 is early, from the center beta of the period of "L", respectively. That is, even if the duty of the clock S1 is not 50%, the clock S2 changes by the same duty as the clock S1, and 90-degree delay is performed.
[0048]Embodiment 2. drawing 9 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 2 of composition of the phase detector circuit 102.
[0049]The phase detector circuit 102 is provided with about 90 degrees of followings.
EXOR sections 13a and 13b.
Current control 14a and 14b.
Only when the clock S1 and the exclusive OR of S2 are "H", it flows through the EXOR section 13a, and only when the clock S1 and the exclusive OR of S2 are "L", it flows through the EXOR section 13b.
[0050]The EXOR section 13a is specifically provided with Pch transistor MP3 [of the characteristic] - MP6, Transistor MP3 and the sauce of MP5 are connected common to the drain of transistor MP0, and transistor MP3 and the drain of MP5 are connected to the sauce of transistor MP4 and MP6, respectively. The drains of transistor MP4 and MP6 are connected. That is, it is connected in parallel mutually and transistor MP3, the series connection body P1 which MP4 constitutes, and the series connection body P2 which transistor MP5 and MP6 constitute constitute the EXOR section 13a. The series connection body N3 and N4 which were shown by Embodiment 1 are connected in parallel mutually, and the EXOR section 13b is constituted.
[0051]In the gate of transistor MP6 and MN5, in common the clock S1, The clock S2 is given to transistor MP3 and the gate of MN6, and the inversion signal S2B is given to the gate of transistor MP4 and MN7 for the inversion signal S1B at the gate of transistor MP5 and MN8,

respectively.
[0052]The current control 14a comprises Pch transistor MP0, power-supply-potential V_D is given to the sauce of transistor MP0, bias potential V_{BP} is given to a gate, respectively, and transistor MP3 and the sauce of MP5 are connected to a drain in common. The current control 14b comprises Nch transistor MN9, the sauce of transistor MN9 is grounded, bias potential V_{BN} is given to a gate, and the sauce of transistor MN6 and MN8 is connected to a drain in common.
[0053]And UP / DOWN signal S3 is acquired from the node W to which the drain of transistor MP4, MP6, MN5, and MN7 is connected in common.
[0054]Here, UP / DOWN signal S3 which takes the mode of current to the low pass filter 2 like Embodiment 1 are outputted by giving bias potential V_{BP} and V_{BN}, as current I_1 passed in both transistor MP0 and MN9.
[0055]If the operation is explained, when the clock S1 and S2 will take an equal logical value, the EXOR sections 13a and 13b will be turned off and turned on, respectively. Therefore, current I_1 flows in as UP / DOWN signal S3 from the low pass filter 2. On the other hand, when taking the clock S1 and the logical value from which S2 differs, the EXOR sections 13a and 13b will be turned on and turned off, respectively. Therefore, current I_1 flows into the low pass filter 2 as UP / DOWN signal S3.
[0056]About 90 degrees which used about 90 degrees concerning Embodiment 2 of phase detector circuits 102 in a phase shifter. It adds to the effect at the time of adopting about 90 degrees concerning Embodiment 1 of phase detector circuits 101, Since the Pch transistor constituted all the high potential sides from the point which takes out UP / DOWN signal S3, all the low potential sides were constituted from a Nch transistor and what is called CMOS structure is taken, circuit structure is further reducible. And in the phase detector circuit 101, the current which was flowing in between between power-supply-potential V_D and grounding is almost lost, and about 90 degrees of effects that power consumption can be reduced are also always added.
[0057]Embodiment 3. drawing 10 is a circuit diagram showing about 90 degrees concerning the embodiment of the invention 3 of principal parts of a phase shifter. The composition of this embodiment is obtained by adding the offset cancel circuit 3 to the composition shown by Embodiment 1.
[0058]The offset cancel circuit 3 generates the offset cancellation signal S5 based on delay control signal S4 obtained from the low pass filter 2. The offset cancellation signal S5 adjusts the value of the resistance R3 which the delay control circuit 50 of the delay stage 5 has.
[0059]The node K to which about 90 degrees of drains of transistor MP1, MN1, MN3, and MN10 were connected in common in the phase detector circuit 101 when a phase locked to the clock S1 in the clock S2 (namely, when a balance is reached). Potential must be almost equal by the node L to which the drain of transistor MP2, MN5, MN7, and MN11 was connected in common.
[0060]However, when there is a difference slightly with temperature etc., since the potential of the drain of transistor MN10 and MN11 differs, few differences will arise on the current which both transistors send. As a result, the mirror efficiency of the current mirror circuit which comprises transistor MN10 and MN11 may fall, and the delay value of the delay stage 5 may reach a balance with a certain amount of phase offset from 90 degrees. And since the balance was reached, while the potential of the nodes K and L carried out neither a rise nor descent but phase offset had been maintained, about 90 degrees of the phase detector circuits 101 will continue operating.
[0061]The offset cancel circuit 3 is formed in order to delay 90 degrees of phases much more

correctly. In the offset cancel circuit 3, the resistance R2 receives delay control signal S4 in the one end, and, as for the other end, one end of capacitor CP2 and the plus input end of the differential amplifier 30 are connected in the node C. The other end of capacitor CP2 is grounded. In the node D, the drain of transistor MP21 and MN20 is connected to the negative input terminal of the differential amplifier 30 in common, and an outgoing end outputs the offset cancellation signal S5. Power-supply-potential V_D is given to the sauce of transistor MP21, and the sauce of transistor MN20 is grounded. The gate and drain of transistor MN20 are connected in common, and bias potential V_{BP} is given to the gate of transistor MP21. The characteristic of transistor MP21 and MN20 is arranged identically to transistor MP1 and MN10 here, respectively, and transistor MP21 and MN20 are provided as a straw man, if transistor MP1 of the phase detector circuit 101 and MN10 say about 90 degrees.

[0062]The differential amplifier 30 receives the potential of the node L in the node C indirectly, and compares it with the potential of the node D. Since it is thought that the potential of the node D is equal to the potential of the node K, the offset cancellation signal S5 can adjust the value of the resistance R3 so that the potential difference of the nodes K and L may be canceled.

[0063]The potential of the node L is transmitted to the node C via two low pass filters with low pass filter 2b which comprises the low pass filter 2, and the resistance R2 and CP2. The low pass filter 2 equalizes the quantity of the electric charge which flows through the node L by capacitor CP1, and generates delay control signal S4 which is a direct-current voltage signal by that cause. After the delay stage 5 is controlled by this signal S4, a new equilibrium situation arises and the potential of the node L also changes in connection with it. By making the damping time constant of low pass filter 2b here larger than the damping time constant of the low pass filter 2 by setting up the value of capacitor CP2 more greatly than the value of capacitor CP1. Change of the potential of the node C which is an output of low pass filter 2b can be made slower than change of the potential of the node L which is an input of the low pass filter 2. The differential amplifier 30 controlling the resistance of the resistance R3 slowly, and maintaining an equilibrium situation mostly, once delay is controlled by taking such composition. The gate potential (that is, potential of the outgoing end of the low pass filter 2) of transistor MN12 can become equal to the potential of the node D.

[0064]Incidentally, since transistor MP21 and MN20 work as a straw man of transistor MP1 and MN10, As the signal from the node L passed two low pass filters and has resulted in the node C, concern whether 2 sets of low pass filters are necessities may arise in the node D. However, since it becomes the value with same current which flows into the low pass filter 2 and current flowing out from the node L when it is in an equilibrium situation, it can be said that it is in the state where it sees on the average in the gate of transistor MN12, and current does not flow with the function of the low pass filter 2. That is, the voltage drop by current flowing also into the resistance R2 connected to the node C is not produced. On the other hand, since the node D is connected to a negative input terminal with a high input impedance called the differential amplifier 30, current does not flow. Therefore, it is not necessary to provide 2 sets of low pass filters to the node D.

[0065]Drawing 11 is a circuit diagram which illustrates the composition of the resistance R3. The resistance R3 is constituted by the fixed resistance R4 and the series connection of Nch transistor MN16. The offset correction signal S5 is given to the gate potential of transistor MN16, and the ON resistance of transistor MN16 is changed.

[0066]As mentioned above, since feedback which controls the current which detects the potential difference of the nodes K and L by the nodes C and D indirectly, and transistor MN12 sends

based on the potential difference by this embodiment is performed, At the time of a lock, the potential of the node L can be mostly coincided with the potential of the node K, and the problem of phase offset can be solved.

[0067]Embodiment 4. drawing 12 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 4 of composition of the phase detector circuit 103. The phase detector circuit 103 has about 90 degrees of composition which replaced the current control [in / about 90 degrees / the phase detector circuit 101] 14 shown in Embodiment 1 by the current control 15.

[0068]The current control 15 is provided with two Nch transistor MN14 and the composition which added 15 to the current control 14. Specifically in the node E, the drain of transistor MP1 and the drain of transistor MN14 are connected for the drain of transistor MN10, the sauce of transistor MN14, and a backgate in the node A, respectively. In the node F, the drain of MP2 and the drain of transistor MN15 are connected for the drain of transistor MN11, the sauce of transistor MN15, and a backgate in the node B, respectively. The EXOR section 13 is connected to the nodes E and F. That is, transistor MP2 as one current source and MN15 can be grasped for transistor MP1 and MN14 as other one current source, respectively.

[0069]In such composition, the potential difference between the node E and the node F can be suppressed as follows by giving bias potential V_{BN2} common to the gate of transistor MN14 and MN15.

[0070]Each potential of the node A, the node B, the node E, and the node F is set to Va, Vb, Ve, and Vf, respectively. While the circuit of drawing 12 is operating, the current which always goes to a ground via any one of the four series connection bodies N1-N4 which constitute the EXOR section 13 is flowing, and the values of the current in the node E and the node F differ momentarily. However, when it sees on the average, if it is in an equilibrium situation, it can be said that the current which flows towards the EXOR section 13 also from the node F becomes the same value also from the node E. Although the current which flows into the low pass filter 2 is also one of an inflow and the outflows from the node B momentarily, current will not flow into the low pass filter 2 on the average.

[0071]Then, the current which flows into transistor MN14 and MN15 will be averaged, and will be equal. This current is made into I_0'. Therefore, several 1 and several 2 are realized (for example, "analogue integrated circuit engineering (second edition) upper written by gray & Maier" Baifukan, p.62 reference).

[0072]

[Equation 1]

$$I_0' = \frac{k}{2}\frac{W}{L}(V_{BN2} - Ve - V_{TH})^2(1 + \lambda(Va - Ve))$$

[0073]

[Equation 2]

$$I_0' = \frac{k}{2}\frac{W}{L}(V_{BN2} - Vf - V_{TH})^2(1 + \lambda(Vb - Vf))$$

[0074]However, k shows the product of gate capacitance and the mobility of an electric charge, as for W and L, the gate width of a transistor, gate length, and V_{TH} show the threshold voltage of a transistor, and lambda shows the short channel effect, respectively. Since the sauce and backgate potential of transistor MN14 and MN15 are equal, the difference of the threshold by the

substrate effect of the transistors MN14 and MN15 has been disregarded.
[0075]Several 1 and several 2 are rewritten as $V_f=V_e+\text{deltaV}_{ef}$ and $V_b=V_a+\text{deltaV}_{ab}$, [0076]
[Equation 3]

$$I_O' = \frac{k}{2}\frac{W}{L}(V_{BN2}-V_e-V_{TH})^2(1+\lambda(V_a-V_e))$$

[0077]
[Equation 4]

$$I_O' = \frac{k}{2}\frac{W}{L}(V_{BN2}-V_e-V_{TH}-\delta V_{ef})^2(1+\lambda(V_a-V_e-\delta V_{ef}+\delta V_{ab}))$$

[0078]******. The following expressions of relations are called for by taking further several 3 and several 4 difference, and disregarding the product of deltaV_{ab} and deltaV_{ef}, or the paragraph of each square.
[0079]
[Equation 5]

$$\frac{\delta V_{ef}}{\delta V_{ab}} = \frac{\lambda(V_{BN2}-V_e-V_{TH})}{2(1+\lambda(V_a-V_e))+\lambda(V_{BN2}-V_e-V_{TH})}$$

[0080]According to the above-mentioned literature, since lambda usually has a value of 0.03 - $0.005V^{-1}$, several 5 value turns into 1/100 or less value.
[0081]Even if this node B to which the phase detector circuit 103 reaches an equilibrium situation, and outputs about 90 degrees of UP / DOWN signals S3 from the above thing differs from potential of the node A used as it and a pair, Between the node E which is a drain part of transistor MN10 which constitutes a current mirror, and MN11, and the node F, it turns out that there can almost be no potential difference. Therefore, current which flows through both transistors can be coincided and about 90 degrees of offset of the phase detector circuit 103 can be controlled.
[0082]Embodiment 5. drawing 13 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 5 of composition of the phase detector circuit 104. The phase detector circuit 103 has about 90 degrees of composition which replaced the current control [in / about 90 degrees / the phase detector circuit 103] 15 shown in Embodiment 4 by the current control 16.
[0083]The current control 16 is provided with composition which added two Pch transistorMP9 and MP 10 to the current control 15. Specifically in the node G, a drain of transistor MP9 and a drain of transistor MN14 are connected for sauce and a backgate of drain [of transistor MP1], and transistor MP9 in the node A, respectively. In the node H, a drain of MP10 and a drain of transistor MN15 are connected for sauce and a backgate of drain [of transistor MP2], and transistor MP10 in the node B, respectively. That is, transistor MP2 as one current source, MP10, and MN15 can be grasped for transistor MP1, MP9, and MN14 as other one current source, respectively.
[0084]In such composition, bias potential V_{BP2} is given common to a gate of transistor MP9 and MP10. In the current control 15 shown in Embodiment 4, when potential difference is between the node A and the node B, a difference will also produce a little current which flows through transistor MP1 and MP2 by the difference in drain voltage. However, since potential difference between the node G of the current control 16 and the node H can be controlled by inserting

transistor MP9 and MP10 by the principle same in this embodiment as Embodiment 4, a still highly precise offset cancel effect is realizable.
[0085]
[Effect of the Invention]Since according to the phase shifter about 90 degrees which claim 1 costs among this invention of the 2nd current is drawn out by the 1st portion from the 1st node when taking the logic from which the 1st and 2nd signals differ, current only with few parts of the 2nd current than the 1st current flows into the 2nd course of a current mirror circuit. On the other hand, since the 2nd current source supplies the 1st current to the 2nd node, the 2nd current flows out of the 2nd node into the 1st low pass filter. Conversely, when the 1st and 2nd signals take equal logic, the 2nd current is drawn out by the 2nd portion from the 2nd node. However, current is not drawn out from the 1st node but the 1st current is flowing into the 2nd course of a current mirror circuit. Therefore, the 2nd current flows into the 2nd node from the 1st low pass filter. It integrates with the outflow ON of such current in the 1st low pass filter, and it controls the delaying amount of a delay part. Since the 1st signal is delayed in a delay part and the 2nd signal is generated, feedback control is performed so that the 1st signal and the 2nd signal may maintain and lock 90-degree phase contrast.
[0086]According to the phase shifter, it flows out of the 2nd node to the 1st low pass filter, and about 90 degrees which claim 2 costs among this invention of jitters of the 2nd current that carries out ON are controlled with the damping time constant determined by the 1st capacitor and resistance.
[0087]According to the phase shifter, by making output potential of the 1st low pass filter into a big value in an initial state, the delay value for acquiring the 2nd signal can be made small, and about 90 degrees which claim 3 costs among this invention of transition operation to a lock can be performed.
[0088]According to the phase shifter, about 90 degrees which claim 4 costs among this invention of values of the 1st and 2nd nodes can be monitored by the dummy part and the 1st low pass filter, respectively. Therefore, even if potential difference arises in the 1st and 2nd nodes and it reaches an equilibrium situation, a control signal can control a delaying amount to control the difference.
[0089]A phase shift can be controlled a differential amplifier controlling the resistance of a variable resistor slowly, and maintaining mostly about 90 degrees which claim 5 costs among this invention of equilibrium situations according to the phase shifter, once delay is controlled.
[0090]Since the 1st transistor of the 1st current source and the 1st transistor of the 2nd current source make small about 90 degrees which claim 6 costs among this invention of potential difference of the 1st node and the 2nd node according to the phase shifter, operation of a current mirror circuit can be ensured and phase offset can be controlled.
[0091]According to the phase shifter, the 3rd transistor of the 1st current source and the 3rd transistor of the 2nd current source can ensure operation of a current mirror circuit further, and can control further about 90 degrees which claim 7 costs among this invention of phase offset.
[0092]According to what starts claim 8 among this invention, based on the 1st and 2nd signals, the 1st switch determines whether the 1st current source is connected as an output node, but the load of the 1st and 2nd signals is equal to the 1st switch. Although the 2nd switch determines whether the 2nd current source is connected as an output node based on the 1st and 2nd signals, the load of the 1st and 2nd signals is equal also to the 2nd switch. Therefore, load about the 1st and 2nd signals can be equalized, and phase offset can be controlled.

TECHNICAL FIELD

[Field of the Invention]This inventions are insides, such as a digital disposal circuit, for example, the receiving circuit of a radio signal, and a processing circuit of a computer, and relate to the delay circuit (in this application, this is called a phase shifter about 90 degrees) outputted so that the inputted signal may be made into 1/4 of the cycle, and a phase and it may become 90-degree delay.

PRIOR ART

[Description of the Prior Art]Drawing 14 is a timing chart which shows a relation with the clock S1 which changes to the same timing as the cycle of transition of the data S6, and transition of the data S6, and a phase. In the digital disposal circuit which receives such the data S6 and the clock S1, The way things stand, when the clock S1 changes, the data S6 has changed, and the data S6 cannot be latched appropriately to latch the data S6 using the standup of the clock S1, or transition of falling. Then, it will be necessary to shift the phase of the clock S1 to the data S6.
[0003]Drawing 15 is the timing chart which made the phase timing to which the clock S1 changes to the timing to which the data S6 changes, and was able to shift it 90 degrees. By doing in this way, the standup of the clock S1 or the timing of falling serves as a center (center of the timing of transition that the data S6 adjoins) of the eye pattern of the data S6, and the latch of the data S6 using transition of the clock S1 becomes the most certain.
[0004]Drawing 16 is a circuit diagram showing the outline of the input interface of the chip 91 which inputs the data S6 and the clock S1. Respectively the data S6 and the clock S1 spread the transmission lines 110a and 110b of the chip 91 exterior, result in the pad electrodes 111a and 111b of chip 91 inside, and are buffered by the buffers 112a and 112b, respectively. The 90-degree phase shift of about 90 degrees of the clocks S1 is carried out by the phase shifter 200 after that, and the clock S2 is generated.
[0005]The data S6 buffered by any data-input-terminals D of the latch circuitry 113a and 113b is given, and the clock S2 is given to which clocked into end T. However, the latch circuitry 113a latches the data S6 at the time of the standup of the clock S2, and the latch circuitry 113b latches the data S6 at the time of falling of the clock S2.
[0006]Drawing 17 is a circuit diagram which illustrates about 90 degrees of composition of the phase shifter 200. The phase shifter 200 is provided with about 90 degrees of the PLL (Phase-LockedLoop) circuits 120 and the delay stages 5. PLL circuit 120 is provided with VCO circuit 122, the phase comparator 121, and the low pass filter 2. Signal S9 by which the reference signal S7 and the phase were locked is generated by this PLL circuit 120. In this case, delay control signal S4 obtained from the low pass filter 2 is adopted as the delay control of the delay stage 5, and the clock S1 buffered by the buffer 112b is in 90 degrees in the delay stage 5, and turns into the output clock S2.
[0007]the time of PLL circuit 120 locking about 90 degrees by the phase shifter 200 -- delay in VCO circuit 122 -- the cycle of the reference signal S7 -- so that it may become half (a phase is used and it is 180 degrees) exactly, Delay control signal S4 from the number and the low pass filter 2 of the buffer 4 of VCO circuit 122 inside is set up. And the output of the couple from the buffer 4 of a final stage carries out a positive/negative inversion, and is connected to the input of the couple of the buffer 4 of the stage at first. By this, when the reference signal S7 is given, VCO circuit 122 will be stabilized and will be oscillated, and signal S9 locked with the same

cycle as the reference signal S7 and the phase will be obtained.
[0008]Then, the signal shifted only one fourth of cycles to the clock S1 is generable as the clock S2 by adopting the clock S1 as the reference signal S7, and having the buffer 4 of the half of the number of the internal buffers 4 with which the delay stage 5 constitutes VCO circuit 122. That is, as long as PLL circuit 120 locks, the delay produced in the delay stage 5 is not dependent on a process or other conditions, is made into a phase, and is held at 90 degrees.

EFFECT OF THE INVENTION

[Effect of the Invention]Since according to the phase shifter about 90 degrees which claim 1 costs among this invention of the 2nd current is drawn out by the 1st portion from the 1st node when taking the logic from which the 1st and 2nd signals differ, current only with few parts of the 2nd current than the 1st current flows into the 2nd course of a current mirror circuit. On the other hand, since the 2nd current source supplies the 1st current to the 2nd node, the 2nd current flows out of the 2nd node into the 1st low pass filter. Conversely, when the 1st and 2nd signals take equal logic, the 2nd current is drawn out by the 2nd portion from the 2nd node. However, current is not drawn out from the 1st node but the 1st current is flowing into the 2nd course of a current mirror circuit. Therefore, the 2nd current flows into the 2nd node from the 1st low pass filter. It integrates with the outflow ON of such current in the 1st low pass filter, and it controls the delaying amount of a delay part. Since the 1st signal is delayed in a delay part and the 2nd signal is generated, feedback control is performed so that the 1st signal and the 2nd signal may maintain and lock 90-degree phase contrast.
[0086]According to the phase shifter, it flows out of the 2nd node to the 1st low pass filter, and about 90 degrees which claim 2 costs among this invention of jitters of the 2nd current that carries out ON are controlled with the damping time constant determined by the 1st capacitor and resistance.
[0087]According to the phase shifter, by making output potential of the 1st low pass filter into a big value in an initial state, the delay value for acquiring the 2nd signal can be made small, and about 90 degrees which claim 3 costs among this invention of transition operation to a lock can be performed.
[0088]According to the phase shifter, about 90 degrees which claim 4 costs among this invention of values of the 1st and 2nd nodes can be monitored by the dummy part and the 1st low pass filter, respectively. Therefore, even if potential difference arises in the 1st and 2nd nodes and it reaches an equilibrium situation, a control signal can control a delaying amount to control the difference.
[0089]A phase shift can be controlled a differential amplifier controlling the resistance of a variable resistor slowly, and maintaining mostly about 90 degrees which claim 5 costs among this invention of equilibrium situations according to the phase shifter, once delay is controlled.
[0090]Since the 1st transistor of the 1st current source and the 1st transistor of the 2nd current source make small about 90 degrees which claim 6 costs among this invention of potential difference of the 1st node and the 2nd node according to the phase shifter, operation of a current mirror circuit can be ensured and phase offset can be controlled.
[0091]According to the phase shifter, the 3rd transistor of the 1st current source and the 3rd transistor of the 2nd current source can ensure operation of a current mirror circuit further, and can control further about 90 degrees which claim 7 costs among this invention of phase offset.
[0092]According to what starts claim 8 among this invention, based on the 1st and 2nd signals,

the 1st switch determines whether the 1st current source is connected as an output node, but the load of the 1st and 2nd signals is equal to the 1st switch. Although the 2nd switch determines whether the 2nd current source is connected as an output node based on the 1st and 2nd signals, the load of the 1st and 2nd signals is equal also to the 2nd switch. Therefore, load about the 1st and 2nd signals can be equalized, and phase offset can be controlled.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, generally there was a problem of the increase of hard quantity and the increase of power consumption which are produced from being a problem of destabilization and VCO being required in a PLL circuit.
[0010]It is going to solve this problem and the art of performing a 90-degree phase shift without using PLL circuit 120 is also proposed. Drawing 18 is a circuit diagram which illustrates about 90 degrees used about 90 degrees in drawing 16 replacing by the phase shifter 200 of composition of the phase shifter 201. The composition of the phase shifter 201 removes about 90 degrees of VCO circuits 122 under composition of the phase shifter 200, and has about 90 degrees of composition which transposed about 90 degrees of phase comparators 121 to the phase detector circuit 100. That is, the phase shifter 201 constitutes about 90 degrees of DLL (Delay-Locked Loop) circuits.
[0011]Drawing 19 is a circuit diagram which illustrates about 90 degrees of composition of the phase detector circuit 100. The phase detector circuit 100 is provided with about 90 degrees of EXOR circuits 10a and the charge pump circuits 11.The clock S1 and the exclusive OR of S2 which were acquired by EXOR circuit 10a are changed into UP / DOWN signal S3 which takes the mode of current in the charge pump circuit 11. In order to supply UP / DOWN signal S3, the current source as which a current amount is determined by a bias signal, respectively is provided in the charge pump circuit 11.
[0012]UP / DOWN signal S3 is given to the low pass filter 2, the current amount integrates with it, it is changed into a direct-current voltage signal, and delay control signal S4 to the delay stage 5 is obtained. Feedback is hung by this delay control signal S4 to the delay for obtaining the clock S2 from the clock S1.
[0013]However, it receives that the clock S1 passes a transfer gate or a NOT circuit, and reaches the charge pump circuit 11 in EXOR circuit 10a, Since the clock S2 is only applied to the gate which manages ON/OFF of a transfer gate, the clock S1 and S2 will receive different input load in EXOR circuit 10a. For this reason, there was a problem that the clock S2 will balance with the phase [degrees / 90] shifted to the clock S1 (below, this gap is called phase offset).
[0014]In order to solve this, adopting EXOR circuit 10b constituted like drawing 20 instead of EXOR circuit 10a is also considered. Although the clock S1 and the input load to S2 become equal with this composition, since the compound gate is used, many transistor counts will be needed, and the problem that circuit structure becomes large will arise.
[0015]It was made in order that this invention might solve the above-mentioned problem, and it aims at obtaining about 90 degrees with easy circuitry of phase shifters. It aims also at obtaining the phase shifter which equalized load about the signal which is two by which a phase should be locked. It aims also at the improvement of phase offset.

MEANS

[Means for Solving the Problem]What starts claim 1 among this invention The 1st and 2nd nodes, The 1st current source that supplies the 1st current to said 1st node, and the 2nd current source that supplies said 1st current to said 2nd node, The 1st current control circuit that has a current mirror circuit including the 1st course that draws out current from said 1st node, and the 2nd course that draws out current from said 2nd node, The 1st portion that draws out the 2nd current from said 1st node only when exclusive OR of the 1st and 2nd signals takes the 1st logic, The 2nd current control circuit that has the 2nd portion that draws out said 2nd current from said 2nd node only when exclusive OR of said 1st and 2nd signals takes said 1st logic and the 2nd different logic, About 90 degrees provided with the 1st low pass filter connected to said 2nd node and a delay part which delays said 1st signal by a delaying amount controlled by output potential of said 1st low pass filter, and outputs said 2nd signal are a phase shifter.
[0017]The 1st end according to claim 1 by which about 90 degrees of things which start claim 2 among this invention are phase shifters, and said 1st low pass filter was connected to said 2nd node, Resistance which has the 2nd end from which said output potential of said 1st low pass filter is obtained, It has the 1st capacitor that has the 1st end connected to said 1st end of said resistance, and the 2nd end, the 1st end connected to said 2nd end of said resistance, and the 2nd end connected to said 2nd end of said 1st capacitor, and has the 2nd capacitor with larger capacity value than said 1st capacitor.
[0018]The about 90 degrees according to claim 2 of things which start claim 3 among this invention are phase shifters, and said 1st low pass filter is further provided with a current supply source mechanism which makes an initial state of said 2nd capacitor a charging state.
[0019]The plus input end according to claim 1 which about 90 degrees of things which start claim 4 among this invention are phase shifters, and makes an input signal said output potential of said 1st low pass filter, A differential amplifier containing a negative input terminal and an outgoing end which outputs a control signal which controls said delaying amount with said output potential of said 1st low pass filter, Connection equivalent to said 1st course of said 1st current source and said current mirror circuit is made, and it is connected to said negative input terminal of said differential amplifier, and has further an offset cancel circuit which has a dummy part containing a dummy node corresponding to said 1st node.
[0020]The about 90 degrees according to claim 4, it is a phase shifter which starts claim 5 among this invention, and said offset cancel circuit, It is inserted between said 1st low pass filter and said plus input end of said differential amplifier, and has further the 2nd low pass filter with a bigger damping time constant than said 1st low pass filter.
[0021]The about 90 degrees according to claim 1 of things which start claim 6 among this invention are phase shifters, and said 1st current source A drain, The 1st transistor that has sauce and a backgate which were connected common to said 1st node, and a gate where the 1st bias is impressed, Sauce and a drain connected to said drain of said 1st transistor, Have the 2nd transistor that has a gate where the 2nd bias is impressed, and said 2nd current source A drain, The 1st transistor that has sauce and a backgate which were connected common to said 2nd node, and a gate where said 1st bias is impressed, It has the 2nd transistor that has said sauce of said 2nd transistor of said 1st current source, connected sauce, a drain connected to said drain of said 1st transistor of said 2nd current source, and a gate where said 2nd bias is impressed.
[0022]The drain according to claim 6 with which about 90 degrees of things which start claim 7 among this invention are phase shifters, and said 1st current source was connected to said drain of said 1st transistor of said 1st current source, Sauce and a backgate which were connected in common with said drain of said 2nd transistor of said 1st current source, A drain which was

further provided with the 3rd transistor that has a gate where the 3rd bias is impressed and with which said 2nd current source was connected to said drain of said 1st transistor of said 2nd current source, It has further the 3rd transistor that has sauce and a backgate which were connected in common with said drain of said 2nd transistor of said 2nd current source, and a gate where said 3rd bias is impressed.

[0023]What starts claim 8 among this invention The 1st current source and the 2nd current source, The 1st switch that flows only when it is provided between an output node, and said 1st current source and said output node and exclusive OR of the 1st and 2nd signals takes the 1st logic, The 2nd switch that flows only when it is provided between said 2nd current source and said output node and exclusive OR of said 1st and 2nd signals takes said 1st logic and the 2nd different logic, About 90 degrees provided with a low pass filter connected to said output node and a delay part which delays said 1st signal by a delaying amount controlled by output potential of said low pass filter, and outputs said 2nd signal are a phase shifter, Said 1st switch has the 1st and 2nd series connection bodies mutually connected in parallel between said 1st current source and said output node, Have said 2nd switch and the 1st and 2nd series connection bodies mutually connected in parallel between said 2nd current source and said output node said 1st series connection body of said 1st switch, A series connection of the 1st transistor that flows when said 1st signal takes said 1st logic, and the 2nd transistor that flows when said 2nd signal takes said 2nd logic is comprised, The 1st transistor through which said 2nd series connection body of said 1st switch flows when said 1st signal takes said 2nd logic, Comprise a series connection with the 2nd transistor that flows when said 2nd signal takes said 1st logic, and said 1st series connection body of said 2nd switch, The 1st transistor that flows when said 1st signal takes said 1st logic, Comprise a series connection with the 2nd transistor that flows when said 2nd signal takes said 1st logic, and said 2nd series connection body of said 2nd switch, About 90 degrees which comprises a series connection of the 1st transistor that flows when said 1st signal takes said 2nd logic, and the 2nd transistor that flows when said 2nd signal takes said 2nd logic are a phase shifter.

[0024]

[Embodiment of the Invention]Embodiment 1. drawing 1 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 1 of composition of the phase detector circuit 101.

[0025]The phase detector circuit 101 is provided with about 90 degrees of the EXOR sections 13 and the current control 14. The EXOR section 13 comprises the Nch transistors MN1-MN8 of the characteristic, and Nch transistor MN9 mutually. The current control 14 is mutually constituted from the Nch transistors MN10 and MN11 of the characteristic by Pch transistorMP1 of the characteristic, MP2, and each.

[0026]In the EXOR section 13, the drains of transistor MN5 and MN7 are connected in common for the drains of transistor MN1 and MN3, respectively. The sauce of transistor MN3 and the drain of transistor MN4 are connected with the sauce of transistor MN1 for the drain of transistor MN2, respectively. The sauce of transistor MN7 and the drain of transistor MN8 are connected with the sauce of transistor MN5 for the drain of transistor MN6, respectively. And the sauce of transistor MN2, MN4, MN6, and MN8 is connected in common. the clock S1 -- the gate of transistor MN1 and MN5 -- give the inversion signal S1B to the gate of transistor MN3 and MN7, the clock S2 is given to the gate of transistor MN4 and MN6, and the inversion signal S2B is given to the gate of transistor MN2 and MN8, respectively. The drain of transistor MN9 is

connected common to the sauce of transistor MN2, MN4, MN6, and MN8, and the sauce of transistor MN9 is grounded. Bias potential V_{BN} is impressed to the gate of transistor MN9.
[0027]In the current control 14, bias potential V_{BP} is given to the sauce of transistor MP1 and MP2 for power-supply-potential V_D in common at the gate, respectively. The sauce of transistor MN10 and MN11 is grounded in common. With the drain and gate of transistor MN10, the drain of transistor MP1 is connected to the drain of transistor MN1 and MN3 in common in the node K. With the drain of transistor MN11, the drain of transistor MP2 is connected to the drain of transistor MN5 and MN7 in common in the node L. UP / DOWN signal S3 is acquired by the node L as current which flows / flows out.
[0028]In the EXOR section 13, when the clock S1 and S2 take the same logical value, one of transistors turns off by the series connection body N1 which transistor MN1 and MN2 constitute. One of transistors turns off also by the series connection body N2 which transistor MN3 and MN4 constitute similarly. Therefore, the series connection body N1 and N2 turn off the branch by which multiple connection was carried out as a whole. On the other hand, in both the series connection bodies N3 that transistor MN5 and MN6 constitute, when the clock S1 and S2 are High(s), both transistor MN5 and MN6 turn on. In both the series connection bodies N4 that transistor MN7 and MN8 constitute, when the clock S1 and S2 are Low(s), both transistor MN5 and MN6 turn on. Therefore, the series connection body N3 and N4 turn on the branch by which multiple connection was carried out as a whole.
[0029]In taking the clock S1 and the logical value from which S2 differs, in the series connection body N3 and N4, one of transistors turns off and it turns off the series connection body N3 and the branch to which multiple connection of N4 was carried out as a whole. On the other hand, the series connection body N1 and either of N2 turn on.
[0030]As mentioned above, the series connection body N1 and the multiple connection of N2 flow, only when the clock S1 and the exclusive OR of S2 are "H", and the series connection body N3 and the multiple connection of N4 flow, only when the clock S1 and the exclusive OR of S2 are "L."
[0031]Drawing 2 is a circuit diagram showing about 90 degrees in case the clock S1 and S2 take the same logical value of equivalent circuits of the phase detector circuit 101. In a figure, the gate where the upward arrow was added shows that logic"H" is given (also setting on the following drawings the same). Bias potential V_{BP} was impressed equally to the gate of transistor MP1 and MP2, and since power-supply-potential V_D is impressed equally, the drain has required the voltage between sauce gates equal also to which transistor MP1 and MP2. both [for this reason,] transistor MP1 and MP2 -- although -- current I_0 is passed equally.
[0032]Transistor MN10 and MN11 constitute the current mirror circuit, and since the series connection body N1 and the branch to which multiple connection of N2 was carried out are moreover turned off as a whole, current equal to current I_0 which transistor MP1 passes flows into transistor MN10 and MN11. On the other hand, since transistor MN9 passes current I_1 based on bias potential V_{BN}, current I_1 is drawn in the current control 14 as UP / DOWN signal S3 from the path connected to the low pass filter 2. Hereafter, current I_1 calls a down period the period drawn in the current control 14 in this way.
[0033]Drawing 3 is a circuit diagram showing about 90 degrees in the case of taking the clock S1 and the logical value from which S2 differs of equivalent circuits of the phase detector circuit 101. When the path which goes to transistor MN9 has arisen from the drain side of transistor MN10, transistor MP1 passes current I_0 and transistor MN9 is passing current I_1, Current (I_0-I_1) will flow into transistor MN10 and MN11. Since transistor MP2 passes current I_0, current I_1

flows out of the current control 14 into the low pass filter 2 as UP / DOWN signal S3. Hereafter, current I_1 calls a rise period the period which flows into the low pass filter 2 in this way.
[0034]Drawing 4 is the timing chart which also added the clock S1, S2 and contrast attachment, and delay control signal S4 for UP / DOWN signal S3 generated as mentioned above. However, the direction out of which it thinks on the basis of the current control 14, is considered as UP / DOWN signal S3, and current flows into the low pass filter 2 is made positive, and the direction which flows from the low pass filter 2 is made negative. About 90 degrees of this embodiment, since about 90 degrees shown in drawing 18 of phase detector circuits 101 can be replaced and used for the phase detector circuit 100, below, they are explained also with reference to drawing 18.
[0035]Considering the case where adjustment of a phase is started from the state where the delay value of the delay stage 5 is less than 90 degrees, as for about 90 degrees of UP / DOWN signals S3 from the phase detector circuit 101, the direction of a down period becomes longer than a rise period. Therefore, delay control signal S4 produced by integrating with UP / DOWN signal S3 in the low pass filter 2, and changing into the voltage of a direct current falls on the average, although there is some exception in a rise period. Therefore, the delay value of the delay stage 5 increases, and when it amounts to one fourth of cycles, about 90 degrees of the rise periods and down periods of UP / DOWN signal S3 of the phase detector circuit 101 become equal. That is, the phase of the clock S2 balances later than it of the clock S1 90 degrees.
[0036]When the delay value of the delay stage 5 starts adjustment of a phase from a bigger value than 90 degrees, as for UP / DOWN signal S3, the direction of a rise period becomes longer than a down period. Therefore, delay control signal S4 goes up on the average, although there is some exception in a down period, and a delay value causes the decreasing tendency. And the phase of the clock S2 balances later than it of the clock S1 90 degrees like the case of the point.
[0037]Drawing 5 is a circuit diagram which illustrates the composition of the delay stage 5. The delay stage 5 is provided with the delay control circuit 50 and the delay buffer part 51. The delay control circuit 50 is provided with Nch transistor MN12, MN13, Pch transistorMP7 and MP8, and the resistance R3. The sauce of transistor MN12 is grounded via the resistance R3, and the drain is connected common to the drain and gate of transistor MP7. Power-supply-potential V_D is given to the sauce of transistor MP7 and MP8 in common, and the drain of transistor MP8 is connected to the gate and drain of transistor MN13. The sauce of transistor MN13 is grounded.
[0038]Current is supplied to the potential side with the high delay buffer part 51 by the Pch transistor, The plurality of the inverter ("delay inverters" is called in this invention) with which current is drawn out has the composition connected in series with the Nch transistor from the low potential side, and the clock S1 which is the target of delay is given to the delay inverters of the stage at first. Since the transistor which specifies the current supplied to delay inverters constitutes the current mirror circuit with transistor MP8 or MN13, the delaying amount in each delay inverters is determined by the current which flows into transistor MN12. Since delay control signal S4 is given to the gate of transistor MN12, as the delay stage 5 whole, the delaying amount of the delay stage 5 will be controlled by delay control signal S4. Of course, the current which flows into transistor MN12 can change the resistance of the resistance R3, and can also be adjusted.
[0039]Drawing 6 is a circuit diagram which illustrates the composition of the low pass filter 2. One end of capacitor CP0 is connected to the 1st end (end by the side of the left in the figure) of the resistance R1, one end of capacitor CP1 is connected to the 2nd end (end by the side of figure Nakamigi), respectively, and the other end of capacitor CP0 and CP1 is grounded in common.

UP / DOWN signal S3 is given to the 1st end of the resistance R1. The capacity value of capacitor CP0 is set up very small as compared with the capacity value of capacitor CP1.
[0040]Since it is easy, if capacitor CP0 is disregarded and considered, the resistance R1 and capacitor CP1 will mainly be integrated with an inflow/outflow of current I_1 to the low pass filter 2 by UP / DOWN signal S3, it will be mostly changed into the voltage of a direct current, and will obtain delay control signal S4.
[0041]The function of capacitor CP0 makes small change of delay control signal S4 always according [current I_1] to the inflow/flowing out to the low pass filter 2. Speaking qualitatively, controlling the high frequency component (jitter) of current I_1 with the damping time constant determined by capacitor CP0 and the resistance R1, and controlling change of the voltage given to the gate of transistor MN12 of the delay control circuit 50. Since the capacity value of capacitor CP0 is dramatically small as compared with the capacity value of capacitor CP1, it hardly depends for the damping time constant in this case on the value of capacitor CP1. However, it is clear to operation of this embodiment that existence of capacitor CP0 is not indispensable.
[0042]The function to set the potential of capacitor CP1 as power-supply-potential V_D based on the reset signal S8 may be applied to the 2nd end of the resistance R1. If the protective diode D1 in preparation for the case where capacitor CP1 is specifically charged more than power-supply-potential V_D, and the switch SW switch on based on the reset signal S8 are formed in series between the potential point which gives power-supply-potential V_D, and the 2nd end of the resistance R1, the above-mentioned function is realizable. By adding this function, the reset signal S8 can be inputted by an initial state, capacitor CP1 can be charged, and current can be started to transistor MN12 from the maximum and the state where made it pass and the delay value of the delay stage 5 was always made into the minimum.
[0043]As mentioned above, in a phase shifter, since not PLL circuit 120 but DLL circuit 201 was adopted, when the frequency of the oscillating frequency of VCO circuit 122 and the clock S1 has a difference, about 90 degrees realized by this embodiment of things for which an error will be integrated are avoided. Since the clock S1 is only compared with the clock S2 produced by delaying this in DLL circuit 201, the addition of the above errors is not produced but there is an advantage of excelling in stability.
[0044]Control of the phase offset by the difference of input load which had been produced when EXOR circuit 10a of the former [about 90 degrees / section / 13 / of the phase detector circuit 101 / EXOR] adopted as a phase shifter was used about 90 more degrees, Being able to realize by a small transistor count as compared with EXOR circuit 10b by a compound gate, circuit structure does not increase. As compared with the charge pump circuit 11 which about 90 degrees of phase detector circuits 100 need, the circuit structure of the current control is small, or even if the current control 14 of the phase detector circuit 101 is large, there are few about 90 degrees of the differences. Phase offset can be controlled by composition produced by replacing about 90 degrees which constitutes after all about 90 degrees which is a DLL circuit of phase shifters of phase detector circuits [about 90 degrees of] 100 in the phase detector circuit 101, without increasing circuit structure.
[0045]Drawing 7 is a timing chart which shows transition of the clock S2 when the period of "H" of the clock S1 is longer than the period of "L", and drawing 8 is a timing chart which shows transition of the clock S2 when the period of "H" of the clock S1 is shorter than the period of "L." a figure -- inside -- a period -- ** - ** -- respectively -- a clock -- S -- one -- S -- two -- (-- " -- H" -- " -- L -- " --) -- (-- " -- H" -- " -- H" --) -- (-- " -- L -- " -- " -- H" --) -- (-- " -- L -- " -- " --

L -- " --) -- a value -- taking -- a period -- being shown -- **** .
[0046]Since delay control signal S4 is controlled based on the clock S1 and the exclusive OR of S2, when the sum total of period ** and period ** and the sum total of period ** and period ** become equal, the clock S2 is locked to the clock S1. And since the clock S2 is in 90 degrees to transition of the clock S1, each of period ** and ** is made into a phase, a 90-degree period is maintained, the sum total of period ** and period ** is made into a phase, and a 180-degree period is maintained.
[0047]When the period of "H" of the clock S1 is longer than the period of "L", a falling edge is located in the timing that only delta 2 is late, from the center beta of the period of "L" at the timing that only the center alphadelta1 of the period of "H" of the clock S1 of the rising edge of the clock S2 is early, respectively. When the period of "H" of the clock S1 is shorter than the period of "L", As for the rising edge of the clock S2, only delta 3 is located in late timing from the center alpha of the period of "H" of the clock S1, and a falling edge is located in the timing that only delta 4 is early, from the center beta of the period of "L", respectively. That is, even if the duty of the clock S1 is not 50%, the clock S2 changes by the same duty as the clock S1, and 90-degree delay is performed.
[0048]Embodiment 2. drawing 9 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 2 of composition of the phase detector circuit 102.
[0049]The phase detector circuit 102 is provided with about 90 degrees of followings.
EXOR sections 13a and 13b.
Current control 14a and 14b.
Only when the clock S1 and the exclusive OR of S2 are "H", it flows through the EXOR section 13a, and only when the clock S1 and the exclusive OR of S2 are "L", it flows through the EXOR section 13b.
[0050]The EXOR section 13a is specifically provided with Pch transistor MP3 [of the characteristic] - MP6, Transistor MP3 and the sauce of MP5 are connected common to the drain of transistor MP0, and transistor MP3 and the drain of MP5 are connected to the sauce of transistor MP4 and MP6, respectively. The drains of transistor MP4 and MP6 are connected. That is, it is connected in parallel mutually and transistor MP3, the series connection body P1 which MP4 constitutes, and the series connection body P2 which transistor MP5 and MP6 constitute constitute the EXOR section 13a. The series connection body N3 and N4 which were shown by Embodiment 1 are connected in parallel mutually, and the EXOR section 13b is constituted.
[0051]In the gate of transistor MP6 and MN5, in common the clock S1, The clock S2 is given to transistor MP3 and the gate of MN6, and the inversion signal S2B is given to the gate of transistor MP4 and MN7 for the inversion signal S1B at the gate of transistor MP5 and MN8, respectively.
[0052]The current control 14a comprises Pch transistor MP0, power-supply-potential V_D is given to the sauce of transistor MP0, bias potential V_{BP} is given to a gate, respectively, and transistor MP3 and the sauce of MP5 are connected to a drain in common. The current control 14b comprises Nch transistor MN9, the sauce of transistor MN9 is grounded, bias potential V_{BN} is given to a gate, and the sauce of transistor MN6 and MN8 is connected to a drain in common.
[0053]And UP / DOWN signal S3 is acquired from the node W to which the drain of transistor MP4, MP6, MN5, and MN7 is connected in common.

[0054]Here, UP / DOWN signal S3 which takes the mode of current to the low pass filter 2 like Embodiment 1 are outputted by giving bias potential V_{BP} and V_{BN}, as current I_1 passed in both transistor MP0 and MN9.
[0055]If the operation is explained, when the clock S1 and S2 will take an equal logical value, the EXOR sections 13a and 13b will be turned off and turned on, respectively. Therefore, current I_1 flows in as UP / DOWN signal S3 from the low pass filter 2. On the other hand, when taking the clock S1 and the logical value from which S2 differs, the EXOR sections 13a and 13b will be turned on and turned off, respectively. Therefore, current I_1 flows into the low pass filter 2 as UP / DOWN signal S3.
[0056]About 90 degrees which used about 90 degrees concerning Embodiment 2 of phase detector circuits 102 in a phase shifter. It adds to the effect at the time of adopting about 90 degrees concerning Embodiment 1 of phase detector circuits 101, Since the Pch transistor constituted all the high potential sides from the point which takes out UP / DOWN signal S3, all the low potential sides were constituted from a Nch transistor and what is called CMOS structure is taken, circuit structure is further reducible. And in the phase detector circuit 101, the current which was flowing in between between power-supply-potential V_D and grounding is almost lost, and about 90 degrees of effects that power consumption can be reduced are also always added.
[0057]Embodiment 3. drawing 10 is a circuit diagram showing about 90 degrees concerning the embodiment of the invention 3 of principal parts of a phase shifter. The composition of this embodiment is obtained by adding the offset cancel circuit 3 to the composition shown by Embodiment 1.
[0058]The offset cancel circuit 3 generates the offset cancellation signal S5 based on delay control signal S4 obtained from the low pass filter 2. The offset cancellation signal S5 adjusts the value of the resistance R3 which the delay control circuit 50 of the delay stage 5 has.
[0059]The node K to which about 90 degrees of drains of transistor MP1, MN1, MN3, and MN10 were connected in common in the phase detector circuit 101 when a phase locked to the clock S1 in the clock S2 (namely, when a balance is reached). Potential must be almost equal by the node L to which the drain of transistor MP2, MN5, MN7, and MN11 was connected in common.
[0060]However, when there is a difference slightly with temperature etc., since the potential of the drain of transistor MN10 and MN11 differs, few differences will arise on the current which both transistors send. As a result, the mirror efficiency of the current mirror circuit which comprises transistor MN10 and MN11 may fall, and the delay value of the delay stage 5 may reach a balance with a certain amount of phase offset from 90 degrees. And since the balance was reached, while the potential of the nodes K and L carried out neither a rise nor descent but phase offset had been maintained, about 90 degrees of the phase detector circuits 101 will continue operating.
[0061]The offset cancel circuit 3 is formed in order to delay 90 degrees of phases much more correctly. In the offset cancel circuit 3, the resistance R2 receives delay control signal S4 in the one end, and, as for the other end, one end of capacitor CP2 and the plus input end of the differential amplifier 30 are connected in the node C. The other end of capacitor CP2 is grounded. In the node D, the drain of transistor MP21 and MN20 is connected to the negative input terminal of the differential amplifier 30 in common, and an outgoing end outputs the offset cancellation signal S5. Power-supply-potential V_D is given to the sauce of transistor MP21, and the sauce of transistor MN20 is grounded. The gate and drain of transistor MN20 are connected in common, and bias potential V_{BP} is given to the gate of transistor MP21. The characteristic of

transistor MP21 and MN20 is arranged identically to transistor MP1 and MN10 here, respectively, and transistor MP21 and MN20 are provided as a straw man, if transistor MP1 of the phase detector circuit 101 and MN10 say about 90 degrees.
[0062]The differential amplifier 30 receives the potential of the node L in the node C indirectly, and compares it with the potential of the node D. Since it is thought that the potential of the node D is equal to the potential of the node K, the offset cancellation signal S5 can adjust the value of the resistance R3 so that the potential difference of the nodes K and L may be canceled.
[0063]The potential of the node L is transmitted to the node C via two low pass filters with low pass filter 2b which comprises the low pass filter 2, and the resistance R2 and CP2. The low pass filter 2 equalizes the quantity of the electric charge which flows through the node L by capacitor CP1, and generates delay control signal S4 which is a direct-current voltage signal by that cause. After the delay stage 5 is controlled by this signal S4, a new equilibrium situation arises and the potential of the node L also changes in connection with it. By making the damping time constant of low pass filter 2b here larger than the damping time constant of the low pass filter 2 by setting up the value of capacitor CP2 more greatly than the value of capacitor CP1. Change of the potential of the node C which is an output of low pass filter 2b can be made slower than change of the potential of the node L which is an input of the low pass filter 2. The differential amplifier 30 controlling the resistance of the resistance R3 slowly, and maintaining an equilibrium situation mostly, once delay is controlled by taking such composition. The gate potential (that is, potential of the outgoing end of the low pass filter 2) of transistor MN12 can become equal to the potential of the node D.
[0064]Incidentally, since transistor MP21 and MN20 work as a straw man of transistor MP1 and MN10, As the signal from the node L passed two low pass filters and has resulted in the node C, concern whether 2 sets of low pass filters are necessities may arise in the node D. However, since it becomes the value with same current which flows into the low pass filter 2 and current flowing out from the node L when it is in an equilibrium situation, it can be said that it is in the state where it sees on the average in the gate of transistor MN12, and current does not flow with the function of the low pass filter 2. That is, the voltage drop by current flowing also into the resistance R2 connected to the node C is not produced. On the other hand, since the node D is connected to a negative input terminal with a high input impedance called the differential amplifier 30, current does not flow. Therefore, it is not necessary to provide 2 sets of low pass filters to the node D.
[0065]Drawing 11 is a circuit diagram which illustrates the composition of the resistance R3. The resistance R3 is constituted by the fixed resistance R4 and the series connection of Nch transistor MN16. The offset correction signal S5 is given to the gate potential of transistor MN16, and the ON resistance of transistor MN16 is changed.
[0066]As mentioned above, since feedback which controls the current which detects the potential difference of the nodes K and L by the nodes C and D indirectly, and transistor MN12 sends based on the potential difference by this embodiment is performed, At the time of a lock, the potential of the node L can be mostly coincided with the potential of the node K, and the problem of phase offset can be solved.
[0067]Embodiment 4. drawing 12 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 4 of composition of the phase detector circuit 103. The phase detector circuit 103 has about 90 degrees of composition which replaced the current control [in / about 90 degrees / the phase detector circuit

101] 14 shown in Embodiment 1 by the current control 15.
[0068]The current control 15 is provided with two Nch transistor MN14 and the composition which added 15 to the current control 14. Specifically in the node E, the drain of transistor MP1 and the drain of transistor MN14 are connected for the drain of transistor MN10, the sauce of transistor MN14, and a backgate in the node A, respectively. In the node F, the drain of MP2 and the drain of transistor MN15 are connected for the drain of transistor MN11, the sauce of transistor MN15, and a backgate in the node B, respectively. The EXOR section 13 is connected to the nodes E and F. That is, transistor MP2 as one current source and MN15 can be grasped for transistor MP1 and MN14 as other one current source, respectively.
[0069]In such composition, the potential difference between the node E and the node F can be suppressed as follows by giving bias potential V_{BN2} common to the gate of transistor MN14 and MN15.
[0070]Each potential of the node A, the node B, the node E, and the node F is set to Va, Vb, Ve, and Vf, respectively. While the circuit of drawing 12 is operating, the current which always goes to a ground via any one of the four series connection bodies N1-N4 which constitute the EXOR section 13 is flowing, and the values of the current in the node E and the node F differ momentarily. However, when it sees on the average, if it is in an equilibrium situation, it can be said that the current which flows towards the EXOR section 13 also from the node F becomes the same value also from the node E. Although the current which flows into the low pass filter 2 is also one of an inflow and the outflows from the node B momentarily, current will not flow into the low pass filter 2 on the average.
[0071]Then, the current which flows into transistor MN14 and MN15 will be averaged, and will be equal. This current is made into I_0'. Therefore, several 1 and several 2 are realized (for example, "analogue integrated circuit engineering (second edition) upper written by gray & Maier" Baifukan, p.62 reference).
[0072]
[Equation 1]

$$I_0' = \frac{k}{2}\frac{W}{L}(V_{BN2} - Ve - V_{TH})^2(1 + \lambda(Va - Ve))$$

[0073]
[Equation 2]

$$I_0' = \frac{k}{2}\frac{W}{L}(V_{BN2} - Vf - V_{TH})^2(1 + \lambda(Vb - Vf))$$

[0074]However, k shows the product of gate capacitance and the mobility of an electric charge, as for W and L, the gate width of a transistor, gate length, and V_{TH} show the threshold voltage of a transistor, and lambda shows the short channel effect, respectively. Since the sauce and backgate potential of transistor MN14 and MN15 are equal, the difference of the threshold by the substrate effect of the transistors MN14 and MN15 has been disregarded.
[0075]Several 1 and several 2 are rewritten as $V_f=V_e+\text{deltaV}_{ef}$ and $V_b=V_a+\text{deltaV}_{ab}$, [0076]
[Equation 3]

$$I_0' = \frac{k}{2}\frac{W}{L}(V_{BN2} - Ve - V_{TH})^2(1 + \lambda(Va - Ve))$$

[0077]
[Equation 4]

$$Io' = \frac{k}{2}\frac{W}{L}(V_{BN2} - Ve - V_{TH} - \delta Vef)^2(1 + \lambda(Va - Ve - \delta Vef + \delta Vab))$$

[0078]******. The following expressions of relations are called for by taking further several 3 and several 4 difference, and disregarding the product of deltaV$_{ab}$ and deltaV$_{ef}$, or the paragraph of each square.

[0079]

[Equation 5]

$$\frac{\delta Vef}{\delta Vab} = \frac{\lambda(V_{BN2} - Ve - V_{TH})}{2(1 + \lambda(Va - Ve)) + \lambda(V_{BN2} - Ve - V_{TH})}$$

[0080]According to the above-mentioned literature, since lambda usually has a value of 0.03 - 0.005V^{-1}, several 5 value turns into 1/100 or less value.

[0081]Even if this node B to which the phase detector circuit 103 reaches an equilibrium situation, and outputs about 90 degrees of UP / DOWN signals S3 from the above thing differs from potential of the node A used as it and a pair, Between the node E which is a drain part of transistor MN10 which constitutes a current mirror, and MN11, and the node F, it turns out that there can almost be no potential difference. Therefore, current which flows through both transistors can be coincided and about 90 degrees of offset of the phase detector circuit 103 can be controlled.

[0082]Embodiment 5. drawing 13 is a circuit diagram showing about 90 degrees which replaces and is used for the phase detector circuit 100 about 90 degrees shown in drawing 18 among phase shifters about 90 degrees concerning the embodiment of the invention 5 of composition of the phase detector circuit 104. The phase detector circuit 103 has about 90 degrees of composition which replaced the current control [in / about 90 degrees / the phase detector circuit 103] 15 shown in Embodiment 4 by the current control 16.

[0083]The current control 16 is provided with composition which added two Pch transistorMP9 and MP 10 to the current control 15. Specifically in the node G, a drain of transistor MP9 and a drain of transistor MN14 are connected for sauce and a backgate of drain [of transistor MP1], and transistor MP9 in the node A, respectively. In the node H, a drain of MP10 and a drain of transistor MN15 are connected for sauce and a backgate of drain [of transistor MP2], and transistor MP10 in the node B, respectively. That is, transistor MP2 as one current source, MP10, and MN15 can be grasped for transistor MP1, MP9, and MN14 as other one current source, respectively.

[0084]In such composition, bias potential V_{BP2} is given common to a gate of transistor MP9 and MP10. In the current control 15 shown in Embodiment 4, when potential difference is between the node A and the node B, a difference will also produce a little current which flows through transistor MP1 and MP2 by the difference in drain voltage. However, since potential difference between the node G of the current control 16 and the node H can be controlled by inserting transistor MP9 and MP10 by the principle same in this embodiment as Embodiment 4, a still highly precise offset cancel effect is realizable.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a circuit diagram showing the composition of the embodiment of the invention 1.

[Drawing 2]It is a circuit diagram showing operation of the embodiment of the invention 1.
[Drawing 3]It is a circuit diagram showing operation of the embodiment of the invention 1.
[Drawing 4]It is a timing chart which shows operation of the embodiment of the invention 1.
[Drawing 5]It is a circuit diagram showing the composition of the embodiment of the invention 1.
[Drawing 6]It is a circuit diagram showing the composition of the embodiment of the invention 1.
[Drawing 7]It is a timing chart which shows operation of the embodiment of the invention 1.
[Drawing 8]It is a timing chart which shows operation of the embodiment of the invention 1.
[Drawing 9]It is a circuit diagram showing the composition of the embodiment of the invention 2.
[Drawing 10]It is a circuit diagram showing the composition of the embodiment of the invention 3.
[Drawing 11]It is a circuit diagram showing the composition of the embodiment of the invention 3.
[Drawing 12]It is a circuit diagram showing the composition of the embodiment of the invention 4.
[Drawing 13]It is a circuit diagram showing the composition of the embodiment of the invention 5.
[Drawing 14]It is a timing chart which shows a Prior art.
[Drawing 15]It is a timing chart which shows a Prior art.
[Drawing 16]It is a circuit diagram showing a Prior art.
[Drawing 17]It is a circuit diagram showing a Prior art.
[Drawing 18]It is a circuit diagram showing a Prior art.
[Drawing 19]It is a circuit diagram showing a Prior art.
[Drawing 20]It is a circuit diagram showing a Prior art.
[Description of Notations]
A,B,E, F,G,H, and K,L,W Node, I_1, I_0, and I_0' current, 2 2b A low pass filter, 13 and 13a, the 13b EXOR section, 14-16, 14a, and 14b Current control and 5 The delay stage and 30 Differential amplifier, 50 A delay control circuit, 51 delay buffer parts, S1, and S2 Clock, S3 UP / DOWN signal, and S4 [A switch and D1 / A diode, V_{BN}, V_{BN2}, V_{BP}, V_{BP2} bias potential.] A delay control signal, and R1-R3 Resistance, and CP0-CP2 A capacitor and SW

[Translation done.]

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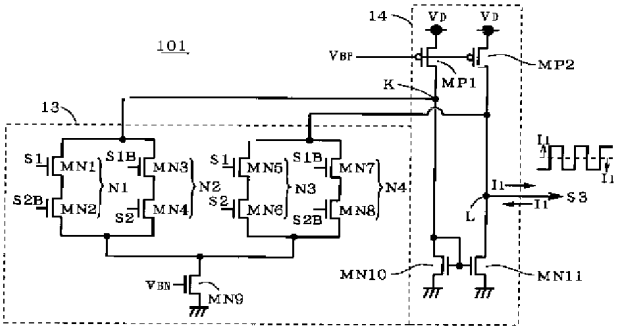
最終頁に続く

(54)【発明の名称】　90°位相シフタ

(57)【要約】
【課題】　入力負荷が均等で、位相オフセットを防ぐ９０°位相シフタを得る。
【解決手段】　トランジスタＭＰ１，ＭＰ２はそれぞれノードＫ，Ｌに電流I_0を供給し、トランジスタＭＮ１０，ＭＮ１１はそれぞれノードＫ，Ｌから互いに等しい電流を引き抜く。直列接続体Ｎ１，Ｎ２の並列接続は、クロックＳ１，Ｓ２の排他的論理和が“Ｈ”のときのみノードＫから電流I_1を引き抜く。一方、直列接続体Ｎ３，Ｎ４の並列接続は、クロックＳ１，Ｓ２の排他的論理和が“Ｌ”のときのみノードＬから電流I_1を引き抜く。ノードＫから電流I_1が引き抜かれれば、ノードＬからは電流I_1が流出し、ノードＬから電流I_1が引き抜かれれば、ノードＬへと電流I_1が流入する。直列接続体Ｎ１～Ｎ４はクロックＳ１，Ｓ２及びそれらの反転信号Ｓ１Ｂ，Ｓ２Ｂをトランジスタ ＭＮ１～ＭＮ８のいずれかのゲートに受けるので、入力負荷は均一になる。



【特許請求の範囲】
【請求項１】　第１及び第２ノードと、
前記第１ノードに第１電流を供給する第１電流源と、
前記第２ノードに前記第１電流を供給する第２電流源と、
前記第１ノードから電流を引き抜く第１経路と、前記第２ノードから電流を引き抜く第２経路とを含むカレントミラー回路とを有する第１電流制御回路と、
第１及び第２信号の排他的論理和が第１論理を採る場合にのみ前記第１ノードから第２電流を引き抜く第１部分と、
前記第１及び第２信号の排他的論理和が前記第１論理と異なる第２論理を採る場合にのみ前記第２ノードから前記第２電流を引き抜く第２部分とを有する第２電流制御回路と、
前記第２ノードに接続された第１ローパスフィルタと、
前記第１ローパスフィルタの出力電位によって制御される遅延量を以て前記第１信号を遅延させて前記第２信号を出力する遅延部とを備える９０°位相シフタ。
【請求項２】　前記第１ローパスフィルタは前記第２ノードに接続された第１端と、前記第１ローパスフィルタの前記出力電位が得られる第２端とを有する抵抗と、
前記抵抗の前記第１端に接続された第１端と、第２端とを有する第１コンデンサと、
前記抵抗の前記第２端に接続された第１端と、前記第１コンデンサの前記第２端に接続された第２端とを有し、前記第１コンデンサよりも容量値が大きい第２コンデンサとを備える、請求項１記載の９０°位相シフタ。
【請求項３】　前記第１ローパスフィルタは前記第２コンデンサの初期状態を充電状態とする電流供給機構を更に備える、請求項２記載の９０°位相シフタ。
【請求項４】　前記第１ローパスフィルタの前記出力電位を入力信号とする正入力端と、負入力端と、前記第１ローパスフィルタの前記出力電位と共に前記遅延量を制御する制御信号を出力する出力端とを含む差動増幅器と、
前記第１電流源及び前記カレントミラー回路の前記第１経路と等価な接続を実現し、前記差動増幅器の前記負入力端に接続され、前記第１ノードに対応するダミーノードを含むダミー部とを有するオフセットキャンセル回路を更に備える、請求項１記載の９０°位相シフタ。
【請求項５】　前記オフセットキャンセル回路は、前記第１ローパスフィルタと前記差動増幅器の前記正入力端との間に介挿され、前記第１ローパスフィルタよりも時定数が大きな第２ローパスフィルタを更に有する、請求項４記載の９０°位相シフタ。
【請求項６】　前記第１電流源はドレインと、前記第１ノードに共通に接続されたソース及びバックゲートと、第１バイアスが印加されるゲートとを有する第１トランジスタと、
ソースと、前記第１トランジスタの前記ドレインに接続されたドレインと、第２バイアスが印加されるゲートとを有する第２トランジスタとを備え、
前記第２電流源はドレインと、前記第２ノードに共通に接続されたソース及びバックゲートと、前記第１バイアスが印加されるゲートとを有する第１トランジスタと、
前記第１電流源の前記第２のトランジスタの前記ソースと接続されたソースと、前記第２電流源の前記第１トランジスタの前記ドレインに接続されたドレインと、前記第２バイアスが印加されるゲートとを有する第２トランジスタとを備えた、請求項１記載の９０°位相シフタ。
【請求項７】　前記第１電流源は前記第１電流源の前記第１トランジスタの前記ドレインに接続されたドレインと、前記第１電流源の前記第２トランジスタの前記ドレインに共通して接続されたソース及びバックゲートと、第３バイアスが印加されるゲートとを有する第３トランジスタを更に備え、
前記第２電流源は前記第２電流源の前記第１トランジスタの前記ドレインに接続されたドレインと、前記第２電流源の前記第２トランジスタの前記ドレインに共通して接続されたソース及びバックゲートと、前記第３バイアスが印加されるゲートとを有する第３トランジスタを更に備える、請求項６記載の９０°位相シフタ。
【請求項８】　第１電流源と、
第２電流源と、
出力ノードと、
前記第１電流源と前記出力ノードとの間に設けられ、第１及び第２信号の排他的論理和が第１論理を採る場合にのみ導通する第１スイッチと、
前記第２電流源と前記出力ノードとの間に設けられ、前記第１及び第２信号の排他的論理和が前記第１論理と異なる第２論理を採る場合にのみ導通する第２スイッチと、
前記出力ノードに接続されたローパスフィルタと、
前記ローパスフィルタの出力電位によって制御される遅延量を以て前記第１信号を遅延させて前記第２信号を出力する遅延部とを備える９０°位相シフタであって、
前記第１スイッチは前記第１電流源と前記出力ノードとの間に互いに並列に接続された第１及び第２直列接続体を有し、
前記第２スイッチは前記第２電流源と前記出力ノードとの間に互いに並列に接続された第１及び第２直列接続体を有し、
前記第１スイッチの前記第１直列接続体は、前記第１信号が前記第１論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第２論理を採る場合に導通する第２トランジスタとの直列接続から成り、
前記第１スイッチの前記第２直列接続体は、前記第１信号が前記第２論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第１論理を採る場合に導通す

る第２トランジスタとの直列接続から成り、
前記第２スイッチの前記第１直列接続体は、前記第１信号が前記第１論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第１論理を採る場合に導通する第２トランジスタとの直列接続から成り、
前記第２スイッチの前記第２直列接続体は、前記第１信号が前記第２論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第２論理を採る場合に導通する第２トランジスタとの直列接続から成る、９０°位相シフタ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、信号処理回路、例えば無線信号の受信回路やコンピュータの処理回路などの内部で、入力された信号をその周期の１／４、位相にして９０°の遅延になるように出力する遅延回路（本願では、これを９０°位相シフタと呼ぶ）に関する。
【０００２】
【従来の技術】図１４は、データＳ６の遷移と、データＳ６の遷移の周期、位相と同じタイミングで遷移するクロックＳ１との関係を示すタイミングチャートである。このようなデータＳ６及びクロックＳ１を受ける信号処理回路において、クロックＳ１の立ち上がりまたは立ち下がりの遷移を用いてデータＳ６をラッチしたい場合、このままではクロックＳ１が遷移する際にはデータＳ６が遷移しており、適切にデータＳ６をラッチすることができない。そこでデータＳ６に対してクロックＳ１の位相をずらす必要が生じる。
【０００３】図１５は、クロックＳ１の遷移するタイミングをデータＳ６の遷移するタイミングに対して位相にして９０°ずらせたタイミングチャートである。このようにすることで、クロックＳ１の立ち上がりまたは立ち下がりのタイミングが、データＳ６のアイパターンの中央（データＳ６の、隣接する遷移のタイミングの中央）となり、クロックＳ１の遷移を用いたデータＳ６のラッチは最も確実となる。
【０００４】図１６は、データＳ６及びクロックＳ１を入力するチップ９１の入力インタフェースの概要を示す回路図である。データＳ６、クロックＳ１はそれぞれ、チップ９１外部の伝送路１１０ａ、１１０ｂを伝搬して、チップ９１内部のパッド電極１１１ａ、１１１ｂに至り、それぞれバッファ１１２ａ、１１２ｂによってバッファリングされる。その後クロックＳ１が９０°位相シフタ２００によって９０°移相され、クロックＳ２が生成される。
【０００５】ラッチ回路１１３ａ、１１３ｂのいずれのデータ入力端Ｄにもバッファリングされたデータ６が与えられ、いずれのクロック入力端Ｔにもクロック２が与えられる。ただし、ラッチ回路１１３ａはクロックＳ２の立ち上がり時にデータＳ６をラッチし、ラッチ回路１１３ｂはクロックＳ２の立ち下がり時にデータＳ６をラッチする。
【０００６】図１７は、９０°位相シフタ２００の構成を例示する回路図である。９０°位相シフタ２００はＰＬＬ（Phase-Locked Loop）回路１２０及び遅延段５を備えている。ＰＬＬ回路１２０はＶＣＯ回路１２２、位相比較器１２１、ローパスフィルタ２を備えている。このＰＬＬ回路１２０により、参照信号Ｓ７と位相がロックされた信号Ｓ９が生成される。この際にローパスフィルタ２から得られる遅延調節信号Ｓ４を遅延段５の遅延調節に採用し、バッファ１１２ｂによってバッファリングされたクロックＳ１は遅延段５で９０°遅れて出力クロックＳ２となる。
【０００７】９０°位相シフタ２００では、ＰＬＬ回路１２０がロックするときにＶＣＯ回路１２２での遅延が、参照信号Ｓ７の周期のちょうど半分（位相にして１８０°）になるように、ＶＣＯ回路１２２内部のバッファ４の数とローパスフィルタ２からの遅延調節信号Ｓ４とが設定される。そして最終段のバッファ４からの一対の出力が正負逆転して最初段のバッファ４の一対の入力へと接続されている。これにより、参照信号Ｓ７を与えたときにＶＣＯ回路１２２は安定して発振し、参照信号Ｓ７と同じ周期、位相でロックした信号Ｓ９を得ることになる。
【０００８】そこで、参照信号Ｓ７としてクロックＳ１を採用し、遅延段５がＶＣＯ回路１２２を構成している内部バッファ４の数の半分のバッファ４を備えることにより、クロックＳ１に対して周期の１／４だけずれた信号をクロックＳ２として生成することができる。つまり遅延段５で生じる遅延は、ＰＬＬ回路１２０がロックしている限りプロセスやその他の条件に依存せず位相にして９０°に保持される。
【０００９】
【発明が解決しようとする課題】しかし、一般にＰＬＬ回路には不安定化の問題や、ＶＣＯが必要なことから生じるハード量の増大や消費電力の増大という問題があった。
【００１０】かかる問題を解消しようとして、ＰＬＬ回路１２０を用いずに９０°の移相を行う技術も提案されている。図１８は図１６において９０°位相シフタ２００と置換されて使用される９０°位相シフタ２０１の構成を例示する回路図である。９０°位相シフタ２０１の構成は、９０°位相シフタ２００の構成中のＶＣＯ回路１２２を除去し、位相比較器１２１を９０°位相検出回路１００に置き換えた構成を有している。つまり、９０°位相シフタ２０１はＤＬＬ（Delay-Locked Loop）回路を構成している。
【００１１】図１９は９０°位相検出回路１００の構成を例示する回路図である。９０°位相検出回路１００はＥＸＯＲ回路１０ａとチャージポンプ回路１１とを備え

ている。ＥＸＯＲ回路１０ａによって得られた、クロックＳ１，Ｓ２の排他的論理和は、チャージポンプ回路１１において電流の態様を採るＵＰ／ＤＯＷＮ信号Ｓ３に変換される。ＵＰ／ＤＯＷＮ信号Ｓ３を供給するために、それぞれバイアス信号によって電流量が決定される電流源がチャージポンプ回路１１に設けられている。

【００１２】ＵＰ／ＤＯＷＮ信号Ｓ３はローパスフィルタ２に与えられてその電流量が積分され、直流的な電圧信号に変換されて遅延段５への遅延調節信号Ｓ４が得られる。この遅延調節信号Ｓ４によって、クロックＳ１からクロックＳ２を得る為の遅延に対してフィードバックが掛けられる。

【００１３】しかしＥＸＯＲ回路１０ａでは、クロックＳ１がトランスファーゲートまたはＮＯＴ回路を通過してチャージポンプ回路１１に至るのに対し、クロックＳ２はトランスファーゲートのＯＮ／ＯＦＦを司るゲートにかかるだけなので、クロックＳ１，Ｓ２はＥＸＯＲ回路１０ａ内で異なる入力負荷を受けることになる。このため、クロックＳ２がクロックＳ１に対して９０°からずれた位相で平衡してしまうという問題があった（このずれのことを以下では位相オフセットと呼ぶ）。

【００１４】これを解決するため、図２０のように構成されたＥＸＯＲ回路１０ｂをＥＸＯＲ回路１０ａの代わりに採用することも考えられる。この構成ではクロックＳ１，Ｓ２に対する入力負荷が等しくなるが、複合ゲートを用いているためにトランジスタ数が多く必要となり、回路規模が大きくなるという問題が生じてしまう。

【００１５】本発明は上記の問題点を解決するためになされたもので、回路構成の簡単な９０°位相シフタを得ることを目的とする。また、位相がロックされるべき２つの信号についての負荷を均等にした位相シフタを得ることをも目的とする。更に、位相オフセットの改善をも目的としている。

【００１６】

【課題を解決するための手段】この発明のうち、請求項１にかかるものは、第１及び第２ノードと、前記第１ノードに第１電流を供給する第１電流源と、前記第２ノードに前記第１電流を供給する第２電流源と、前記第１ノードから電流を引き抜く第１経路と、前記第２ノードから電流を引き抜く第２経路とを含むカレントミラー回路とを有する第１電流制御回路と、第１及び第２信号の排他的論理和が第１論理を採る場合にのみ前記第１ノードから第２電流を引き抜く第１部分と、前記第１及び第２信号の排他的論理和が前記第１論理と異なる第２論理を採る場合にのみ前記第２ノードから前記第２電流を引き抜く第２部分とを有する第２電流制御回路と、前記第２ノードに接続された第１ローパスフィルタと、前記第１ローパスフィルタの出力電位によって制御される遅延量を以て前記第１信号を遅延させて前記第２信号を出力する遅延部とを備える９０°位相シフタである。

【００１７】この発明のうち、請求項２にかかるものは、請求項１記載の９０°位相シフタであって、前記第１ローパスフィルタは前記第２ノードに接続された第１端と、前記第１ローパスフィルタの前記出力電位が得られる第２端とを有する抵抗と、前記抵抗の前記第１端に接続された第１端と、第２端とを有する第１コンデンサと、前記抵抗の前記第２端に接続された第１端と、前記第１コンデンサの前記第２端に接続された第２端とを有し、前記第１コンデンサよりも容量値が大きい第２コンデンサとを備える。

【００１８】この発明のうち、請求項３にかかるものは、請求項２記載の９０°位相シフタであって、前記第１ローパスフィルタは前記第２コンデンサの初期状態を充電状態とする電流供給機構を更に備える。

【００１９】この発明のうち、請求項４にかかるものは、請求項１記載の９０°位相シフタであって、前記第１ローパスフィルタの前記出力電位を入力信号とする正入力端と、負入力端と、前記第１ローパスフィルタの前記出力電位と共に前記遅延量を制御する制御信号を出力する出力端とを含む差動増幅器と、前記第１電流源及び前記カレントミラー回路の前記第１経路と等価な接続を実現し、前記差動増幅器の前記負入力端に接続され、前記第１ノードに対応するダミーノードを含むダミー部とを有するオフセットキャンセル回路を更に備える。

【００２０】この発明のうち、請求項５にかかるものは、請求項４記載の９０°位相シフタであって前記オフセットキャンセル回路は、前記第１ローパスフィルタと前記差動増幅器の前記正入力端との間に介挿され、前記第１ローパスフィルタよりも時定数が大きな第２ローパスフィルタを更に有する。

【００２１】この発明のうち、請求項６にかかるものは、請求項１記載の９０°位相シフタであって、前記第１電流源はドレインと、前記第１ノードに共通に接続されたソース及びバックゲートと、第１バイアスが印加されるゲートとを有する第１トランジスタと、ソースと、前記第１トランジスタの前記ドレインに接続されたドレインと、第２バイアスが印加されるゲートとを有する第２トランジスタとを備え、前記第２電流源はドレインと、前記第２ノードに共通に接続されたソース及びバックゲートと、前記第１バイアスが印加されるゲートとを有する第１トランジスタと、前記第１電流源の前記第２のトランジスタの前記ソースと接続されたソースと、前記第２電流源の前記第１トランジスタの前記ドレインに接続されたドレインと、前記第２バイアスが印加されるゲートとを有する第２トランジスタとを備える。

【００２２】この発明のうち、請求項７にかかるものは、請求項６記載の９０°位相シフタであって、前記第１電流源は前記第１電流源の前記第１トランジスタの前記ドレインに接続されたドレインと、前記第１電流源の前記第２トランジスタの前記ドレインに共通して接続さ

れたソース及びバックゲートと、第３バイアスが印加されるゲートとを有する第３トランジスタを更に備え、前記第２電流源は前記第２電流源の前記第１トランジスタの前記ドレインに接続されたドレインと、前記第２電流源の前記第２トランジスタの前記ドレインに共通して接続されたソース及びバックゲートと、前記第３バイアスが印加されるゲートとを有する第３トランジスタを更に備える。

【００２３】この発明のうち、請求項８にかかるものは、第１電流源と、第２電流源と、出力ノードと、前記第１電流源と前記出力ノードとの間に設けられ、第１及び第２信号の排他的論理和が第１論理を採る場合にのみ導通する第１スイッチと、前記第２電流源と前記出力ノードとの間に設けられ、前記第１及び第２信号の排他的論理和が前記第１論理と異なる第２論理を採る場合にのみ導通する第２スイッチと、前記出力ノードに接続されたローパスフィルタと、前記ローパスフィルタの出力電位によって制御される遅延量を以て前記第１信号を遅延させて前記第２信号を出力する遅延部とを備える９０°位相シフタであって、前記第１スイッチは前記第１電流源と前記出力ノードとの間に互いに並列に接続された第１及び第２直列接続体を有し、前記第２スイッチは前記第２電流源と前記出力ノードとの間に互いに並列に接続された第１及び第２直列接続体を有し、前記第１スイッチの前記第１直列接続体は、前記第１信号が前記第１論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第２論理を採る場合に導通する第２トランジスタとの直列接続から成り、前記第１スイッチの前記第２直列接続体は、前記第１信号が前記第２論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第１論理を採る場合に導通する第２トランジスタとの直列接続から成り、前記第２スイッチの前記第１直列接続体は、前記第１信号が前記第１論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第１論理を採る場合に導通する第２トランジスタとの直列接続から成り、前記第２スイッチの前記第２直列接続体は、前記第１信号が前記第２論理を採る場合に導通する第１トランジスタと、前記第２信号が前記第２論理を採る場合に導通する第２トランジスタとの直列接続から成る、９０°位相シフタである。

【００２４】

【発明の実施の形態】実施の形態１．図１は本発明の実施の形態１にかかる９０°位相シフタのうち、図１８に示された９０°位相検出回路１００に置換して用いられる９０°位相検出回路１０１の構成を示す回路図である。

【００２５】９０°位相検出回路１０１は、ＥＸＯＲ部１３と電流制御部１４とを備えている。ＥＸＯＲ部１３は互いに同特性のＮｃｈトランジスタＭＮ１～ＭＮ８と、Ｎｃｈトランジスタ ＭＮ９とで構成されている。また電流制御部１４は、互いに同特性のＰｃｈトランジスタＭＰ１，ＭＰ２及び互いに同特性のＮｃｈトランジスタＭＮ１０とＭＮ１１で構成されている。

【００２６】ＥＸＯＲ部１３において、トランジスタＭＮ１，ＭＮ３のドレイン同士が、トランジスタＭＮ５，ＭＮ７のドレイン同士が、それぞれ共通に接続されている。またトランジスタＭＮ１のソースとトランジスタＭＮ２のドレインが、トランジスタＭＮ３のソースとトランジスタＭＮ４のドレインが、それぞれ接続されている。またトランジスタＭＮ５のソースとトランジスタＭＮ６のドレインが、トランジスタＭＮ７のソースとトランジスタＭＮ８のドレインが、それぞれ接続されている。そしてトランジスタＭＮ２，ＭＮ４，ＭＮ６，ＭＮ８のソースは共通して接続されている。クロックＳ１はトランジスタＭＮ１，ＭＮ５のゲートに、その反転信号ＳＢはトランジスタＭＮ３，ＭＮ７のゲートに、クロックＳ２はトランジスタＭＮ４，ＭＮ６のゲートに、その反転信号ＳＢはトランジスタＭＮ２，ＭＮ８のゲートに、それぞれ与えられている。トランジスタＭＮ９のドレインはトランジスタＭＮ２，ＭＮ４，ＭＮ６，ＭＮ８のソースに共通に接続され、トランジスタＭＮ９のソースは接地されている。またトランジスタＭＮ９のゲートにはバイアス電位V_{BN}が印加されている。

【００２７】電流制御部１４において、トランジスタＭＰ１，ＭＰ２のソースには共通して電源電位V_Dが、ゲートにはバイアス電位V_{BP}が、それぞれ与えられている。トランジスタＭＮ１０，ＭＮ１１のソースは共通して接地されている。トランジスタＭＰ１のドレインはトランジスタＭＮ１０のドレイン及びゲートと共に、ノードＫにおいてトランジスタＭＮ１，ＭＮ３のドレインに共通に接続されている。またトランジスタＭＰ２のドレインはトランジスタＭＮ１１のドレインと共に、ノードＬにおいてトランジスタＭＮ５，ＭＮ７のドレインに共通に接続されている。ノードＬに流入／流出する電流としてＵＰ／ＤＯＷＮ信号Ｓ３が得られる。

【００２８】ＥＸＯＲ部１３において、クロックＳ１，Ｓ２が同じ論理値を採る場合にはトランジスタＭＮ１，ＭＮ２が構成する直列接続体Ｎ１では何れか一方のトランジスタがＯＦＦする。同様にしてトランジスタＭＮ３，ＭＮ４が構成する直列接続体Ｎ２でも何れか一方のトランジスタがＯＦＦする。従って、直列接続体Ｎ１，Ｎ２が並列接続された枝は全体としてＯＦＦしている。一方、トランジスタＭＮ５，ＭＮ６が構成する直列接続体Ｎ３では、クロックＳ１，Ｓ２が共にＨｉｇｈの場合にトランジスタＭＮ５，ＭＮ６はともにＯＮする。またトランジスタＭＮ７，ＭＮ８が構成する直列接続体Ｎ４では、クロックＳ１，Ｓ２が共にＬｏｗの場合にトランジスタＭＮ５，ＭＮ６が共にＯＮする。従って、直列接続体Ｎ３，Ｎ４が並列接続された枝は全体としてＯＮしている。

【００２９】クロックＳ１，Ｓ２が異なる論理値を採る場合には直列接続体Ｎ３，Ｎ４では何れか一方のトランジスタがＯＦＦし、直列接続体Ｎ３，Ｎ４が並列接続された枝は全体としてＯＦＦしている。一方、直列接続体Ｎ１，Ｎ２のいずれか一方がＯＮする。

【００３０】以上のように、直列接続体Ｎ１，Ｎ２の並列接続はクロックＳ１，Ｓ２の排他的論理和が“Ｈ”の場合にのみ導通し、直列接続体Ｎ３，Ｎ４の並列接続はクロックＳ１，Ｓ２の排他的論理和が“Ｌ”の場合にのみ導通する。

【００３１】図２はクロックＳ１，Ｓ２が同じ論理値を採る場合の９０°位相検出回路１０１の等価回路を示す回路図である。図において、上向きの矢印が付加されたゲートは、論理“Ｈ”が与えられていることを示す（以下の図面においても同様）。トランジスタＭＰ１，ＭＰ２のゲートには等しくバイアス電位V_{BP}が印加され、ドレインは等しく電源電位V_Dが印加されているので、どちらのトランジスタＭＰ１，ＭＰ２にも等しいソース－ゲート間電圧がかかっている。このため、トランジスタＭＰ１，ＭＰ２のいずれもが等しく電流I_0を流す。

【００３２】トランジスタＭＮ１０，ＭＮ１１はカレントミラー回路を構成しており、しかも直列接続体Ｎ１，Ｎ２が並列接続された枝は全体としてＯＦＦしているので、トランジスタＭＰ１が流す電流I_0と等しい電流がトランジスタＭＮ１０，ＭＮ１１に流れる。一方、トランジスタＭＮ９は、バイアス電位V_{BN}に基づいて電流I_1を流すので、ローパスフィルタ２へとつながっているパスから、ＵＰ／ＤＯＷＮ信号Ｓ３として電流I_1が電流制御部１４へと引き込まれる。以下、このように電流I_1が電流制御部１４へと引き込まれる期間をダウン期間と称する。

【００３３】図３はクロックＳ１，Ｓ２が異なる論理値を採る場合の９０°位相検出回路１０１の等価回路を示す回路図である。トランジスタＭＮ１０のドレイン側からトランジスタＭＮ９へ向かうパスが生じており、トランジスタＭＰ１が電流I_0を流し、トランジスタＭＮ９が電流I_1を流していることにより、トランジスタＭＮ１０，ＭＮ１１には電流（I_0-I_1）が流れることになる。トランジスタＭＰ２は電流I_0を流すので、ＵＰ／ＤＯＷＮ信号Ｓ３として電流I_1が電流制御部１４からローパスフィルタ２へと流出する。以下、このように電流I_1がローパスフィルタ２へと流出する期間をアップ期間と称する。

【００３４】図４は、以上のようにして生成されるＵＰ／ＤＯＷＮ信号Ｓ３をクロックＳ１，Ｓ２と対比づけ、遅延調節信号Ｓ４をも追記したタイミングチャートである。但し、電流制御部１４を基準として考えてＵＰ／ＤＯＷＮ信号Ｓ３として電流がローパスフィルタ２へと流出する方向を正とし、ローパスフィルタ２から流入する方向を負としている。本実施の形態の９０°位相検出回路１０１は、図１８に示された９０°位相検出回路１００に置換して用いることができるので、以下では図１８をも参照して説明する。

【００３５】遅延段５の遅延値が９０°未満である状態から位相の調整を開始する場合を考えると、９０°位相検出回路１０１からのＵＰ／ＤＯＷＮ信号Ｓ３はダウン期間の方がアップ期間よりも長くなる。従ってローパスフィルタ２においてＵＰ／ＤＯＷＮ信号Ｓ３を積分して直流の電圧に変換して得られる遅延調節信号Ｓ４は、アップ期間において若干の例外はあるものの、平均的には低下する。よって遅延段５の遅延値は増大し、周期の１／４に達したときに９０°位相検出回路１０１のＵＰ／ＤＯＷＮ信号Ｓ３のアップ期間とダウン期間とは等しくなる。つまり、クロックＳ２の位相がクロックＳ１のそれよりも９０°遅れて平衡する。

【００３６】遅延段５の遅延値が９０°より大きな値から位相の調整を開始する場合には、ＵＰ／ＤＯＷＮ信号Ｓ３はアップ期間の方がダウン期間よりも長くなる。従って遅延調節信号Ｓ４はダウン期間において若干の例外はあるものの、平均的には上昇し、遅延値は減少する傾向を招く。そして先の場合と同様、クロックＳ２の位相がクロックＳ１のそれよりも９０°遅れて平衡する。

【００３７】図５は遅延段５の構成を例示する回路図である。遅延段５は遅延調節回路５０と遅延バッファ部５１とを備えている。遅延調節回路５０はＮｃｈトランジスタＭＮ１２，ＭＮ１３と、ＰｃｈトランジスタＭＰ７，ＭＰ８と、抵抗Ｒ３とを備えている。トランジスタＭＮ１２のソースは抵抗Ｒ３を介して接地されており、ドレインはトランジスタＭＰ７のドレイン及びゲートに共通に接続されている。トランジスタＭＰ７，ＭＰ８のソースには共通して電源電位V_Dが与えられており、トランジスタＭＰ８のドレインはトランジスタＭＮ１３のゲート及びドレインに接続されている。トランジスタＭＮ１３のソースは接地されている。

【００３８】遅延バッファ部５１は高い電位側へとＰｃｈトランジスタによって電流が供給され、低い電位側からＮｃｈトランジスタによって電流が引き抜かれるインバータ（本発明では「遅延インバータ」と称す）の複数が直列に接続された構成を有しており、最初段の遅延インバータには遅延の対象となるクロックＳ１が与えられている。遅延インバータに供給される電流を規定するトランジスタは、トランジスタＭＰ８あるいはＭＮ１３と共にカレントミラー回路を構成しているので、トランジスタＭＮ１２に流れる電流によって各遅延インバータにおける遅延量が決定される。トランジスタＭＮ１２のゲートには遅延調節信号Ｓ４が与えられるので、遅延段５全体としては遅延調節信号Ｓ４によって遅延段５の遅延量が制御されることになる。勿論、トランジスタＭＮ１２に流れる電流は、抵抗Ｒ３の抵抗値を変化させて調節することもできる。

【００３９】図６は、ローパスフィルタ２の構成を例示する回路図である。抵抗Ｒ１の第１端（図中左側の端）にはコンデンサＣＰ０の一端が、第２端（図中右側の端）にはコンデンサＣＰ１の一端が、それぞれ接続されており、コンデンサＣＰ０，ＣＰ１の他端は共通して接地されている。ＵＰ／ＤＯＷＮ信号Ｓ３は抵抗Ｒ１の第１端に与えられる。コンデンサＣＰ０の容量値はコンデンサＣＰ１の容量値と比較して非常に小さく設定される。

【００４０】簡単の為にコンデンサＣＰ０を無視して考えると、ＵＰ／ＤＯＷＮ信号Ｓ３によるローパスフィルタ２への電流I_1の流入／流出は、主として抵抗Ｒ１及びコンデンサＣＰ１で積分され、ほぼ直流の電圧に変換されて遅延調節信号Ｓ４を得る。

【００４１】コンデンサＣＰ０の機能は、電流I_1が常にローパスフィルタ２へ流入／流出していることによる遅延調節信号Ｓ４の変動を小さくするものである。定性的に言えば、電流I_1の高周波成分（ジッタ）をコンデンサＣＰ０と抵抗Ｒ１で決定される時定数で抑制し、遅延調節回路５０のトランジスタＭＮ１２のゲートに与えられる電圧の変動を抑制するのである。この場合の時定数は、コンデンサＣＰ０の容量値がコンデンサＣＰ１の容量値と比較して非常に小さいので、コンデンサＣＰ１の値にはほとんど依存しない。但し、本実施の形態の実施にコンデンサＣＰ０の存在が必須でないことは明白である。

【００４２】なお、抵抗Ｒ１の第２端に対し、リセット信号Ｓ８に基づいてコンデンサＣＰ１の電位を電源電位V_Dに設定する機能を加えてもよい。具体的にはコンデンサＣＰ１が電源電位V_D以上に充電されていた場合に備えての保護ダイオードＤ１と、リセット信号Ｓ８に基づいてＯＮするスイッチＳＷとを電源電位V_Dを与える電位点と抵抗Ｒ１の第２端との間に直列に設ければ上記機能を実現できる。かかる機能を付加することにより、初期状態でリセット信号Ｓ８を入力して、コンデンサＣＰ１を充電し、トランジスタＭＮ１２に電流を最大限、流させ、遅延段５の遅延値を必ず最小にした状態からスタートすることができる。

【００４３】以上のように、本実施の形態によって実現される９０°位相シフタでは、ＰＬＬ回路１２０ではなくＤＬＬ回路２０１を採用したので、ＶＣＯ回路１２２の発振周波数とクロックＳ１との周波数に差がある場合に誤差が積算されてしまうことが回避される。ＤＬＬ回路２０１ではクロックＳ１と、これを遅延して得られるクロックＳ２とを単に比較しているので、上記のような誤差の積算は生じず、安定性に優れるという利点がある。

【００４４】更に９０°位相シフタとして採用する９０°位相検出回路１０１のＥＸＯＲ部１３は従来のＥＸＯＲ回路１０ａを用いた場合に生じていたような入力負荷の差による位相オフセットの抑制を、複合ゲートによるＥＸＯＲ回路１０ｂと比較して少ないトランジスタ数で実現することができ、回路規模は増大しない。また、９０°位相検出回路１０１の電流制御部１４は９０°位相検出回路１００が必要とするチャージポンプ回路１１と比較して回路規模は小さいか、あるいは大きくてもその差は少ない。結局、ＤＬＬ回路である９０°位相シフタを構成する９０°位相検出回路１００を９０°位相検出回路１０１で置換して得られる構成により、回路規模を増大させることなく、位相オフセットを抑制することができる。

【００４５】図７はクロックＳ１の“Ｈ”の期間が“Ｌ”の期間よりも長い場合のクロックＳ２の遷移を示すタイミングチャートであり、図８はクロックＳ１の“Ｈ”の期間が“Ｌ”の期間よりも短い場合のクロックＳ２の遷移を示すタイミングチャートである。図中、期間①～④は、それぞれクロックＳ１，Ｓ２が（“Ｈ”，“Ｌ”），（“Ｈ”，“Ｈ”），（“Ｌ”，“Ｈ”），（“Ｌ”，“Ｌ”）の値を採る期間を示している。

【００４６】クロックＳ１，Ｓ２の排他的論理和に基づいて遅延調節信号Ｓ４が制御されるので、期間① と期間③ の合計と、期間② と期間④ の合計とが等しくなるときにクロックＳ２はクロックＳ１に対してロックする。しかもクロックＳ２はクロックＳ１の遷移に対して９０°遅れるので、期間①，③ はいずれも位相にして９０°の期間が保たれ、期間② と期間④ の合計は位相にして１８０°の期間が保たれる。

【００４７】クロックＳ１の“Ｈ”の期間が“Ｌ”の期間よりも長い場合には、クロックＳ２の立ち上がりエッジはクロックＳ１の“Ｈ”の期間の中心αよりもδ１だけ早いタイミングに、立ち下がりエッジは“Ｌ”の期間の中心βよりもδ２だけ遅いタイミングに、それぞれ位置する。また、クロックＳ１の“Ｈ”の期間が“Ｌ”の期間よりも短い場合には、クロックＳ２の立ち上がりエッジはクロックＳ１の“Ｈ”の期間の中心αよりもδ３だけ遅いタイミングに、立ち下がりエッジは“Ｌ”の期間の中心βよりもδ４だけ早いタイミングに、それぞれ位置する。つまりクロックＳ１のデューティが５０％でなくても、クロックＳ２はクロックＳ１と同じデューティで遷移し、９０°の遅延が行われる。

【００４８】実施の形態２．図９は本発明の実施の形態２にかかる９０°位相シフタのうち、図１８に示された９０°位相検出回路１００に置換して用いられる９０°位相検出回路１０２の構成を示す回路図である。

【００４９】９０°位相検出回路１０２は、ＥＸＯＲ部１３ａ，１３ｂと、電流制御部１４ａ，１４ｂとを備えている。ＥＸＯＲ部１３ａは、クロックＳ１，Ｓ２の排他的論理和が“Ｈ”の場合にのみ導通し、ＥＸＯＲ部１３ｂはクロックＳ１，Ｓ２の排他的論理和が“Ｌ”の場合にのみ導通する。

【００５０】具体的には、ＥＸＯＲ部１３ａは同特性のＰｃｈトランジスタＭＰ３～ＭＰ６を備えており、トランジスタＭＰ３，ＭＰ５のソースが、トランジスタＭＰ０のドレインに共通に接続され、トランジスタＭＰ３，ＭＰ５のドレインはそれぞれトランジスタＭＰ４，ＭＰ６のソースに接続されている。また、トランジスタＭＰ４，ＭＰ６のドレイン同士が接続されている。つまりトランジスタＭＰ３，ＭＰ４が構成する直列接続体Ｐ１と、トランジスタＭＰ５，ＭＰ６が構成する直列接続体Ｐ２とが、互いに並列に接続されてＥＸＯＲ部１３ａを構成している。また、ＥＸＯＲ部１３ｂは、実施の形態１で示された直列接続体Ｎ３，Ｎ４が互いに並列に接続されて構成されている。

【００５１】トランジスタＭＰ６，ＭＮ５のゲートには共通してクロックＳ１が、トランジスタＭＰ４，ＭＮ７のゲートにはその反転信号Ｓ１Ｂが、トランジスタＭＰ３，ＭＮ６のゲートにはクロックＳ２が、トランジスタＭＰ５，ＭＮ８のゲートにはその反転信号Ｓ２Ｂが、それぞれ与えられる。

【００５２】電流制御部１４ａはＰｃｈトランジスタＭＰ０で構成されており、トランジスタＭＰ０のソースには電源電位V_Dが、ゲートにはバイアス電位V_{BP}が、それぞれ与えられ、ドレインにはトランジスタＭＰ３，ＭＰ５のソースが共通して接続される。また電流制御部１４ｂはＮｃｈトランジスタＭＮ９で構成されており、トランジスタＭＮ９のソースは接地され、ゲートにはバイアス電位V_{BN}が与えられ、ドレインにはトランジスタＭＮ６，ＭＮ８のソースが共通して接続される。

【００５３】そしてトランジスタＭＰ４，ＭＰ６，ＭＮ５，ＭＮ７のドレインが共通して接続されるノードＷからＵＰ／ＤＯＷＮ信号Ｓ３が得られる。

【００５４】ここで、トランジスタＭＰ０，ＭＮ９が共に電流I_1を流すようにバイアス電位V_{BP}、V_{BN}を与えることにより、実施の形態１と同様にしてローパスフィルタ２へ電流の態様を採るＵＰ／ＤＯＷＮ信号Ｓ３を出力する。

【００５５】その動作を説明すると、クロックＳ１，Ｓ２が等しい論理値を採る場合には、ＥＸＯＲ部１３ａ，１３ｂはそれぞれＯＦＦ，ＯＮすることになる。よって電流I_1はローパスフィルタ２からＵＰ／ＤＯＷＮ信号Ｓ３として流れ込む。一方、クロックＳ１，Ｓ２が異なる論理値を採る場合には、ＥＸＯＲ部１３ａ，１３ｂはそれぞれＯＮ，ＯＦＦすることになる。よって電流I_1はローパスフィルタ２へとＵＰ／ＤＯＷＮ信号Ｓ３として流れ出す。

【００５６】実施の形態２にかかる９０°位相検出回路１０２を用いた９０°位相シフタでは、実施の形態１にかかる９０°位相検出回路１０１を採用した場合の効果に加えて、ＵＰ／ＤＯＷＮ信号Ｓ３を取り出す点から高い電位側を全てＰｃｈトランジスタで構成し、低い電位側を全てＮｃｈトランジスタで構成し、いわゆるＣＭＯＳ構成を採っているので、回路規模をさらに削減できる。しかも、９０°位相検出回路１０１では常時、電源電位V_Dと接地との間に間に流れていた電流が殆どなくなり、消費電力を低減できるという効果も付加される。

【００５７】実施の形態３．図１０は本発明の実施の形態３にかかる９０°位相シフタの主要部を示す回路図である。本実施の形態の構成は、実施の形態１で示された構成に対してオフセットキャンセル回路３を追加して得られる。

【００５８】オフセットキャンセル回路３はローパスフィルタ２から得られた遅延調節信号Ｓ４に基づいてオフセットキャンセル信号Ｓ５を生成する。オフセットキャンセル信号Ｓ５は、遅延段５の遅延調節回路５０が有する抵抗Ｒ３の値を調節する。

【００５９】９０°位相検出回路１０１において、クロックＳ２がクロックＳ１に対して位相がロックした場合（即ち平衡に達したとき）、トランジスタＭＰ１，ＭＮ１，ＭＮ３，ＭＮ１０のドレインが共通に接続されたノードＫと、トランジスタＭＰ２，ＭＮ５，ＭＮ７，ＭＮ１１のドレインが共通に接続されたノードＬとでは、電位がほぼ等しくなっているはずである。

【００６０】しかし、温度等によりわずかに差がある場合、トランジスタＭＮ１０，ＭＮ１１のドレインの電位が異なることから、両トランジスタが流す電流にわずかな差が生じることになる。この結果、トランジスタＭＮ１０，ＭＮ１１で構成されるカレントミラー回路のミラー効率が低下し、遅延段５の遅延値は９０°からある程度の位相オフセットを持って平衡に達する場合がある。そして平衡に達しているためノードＫ，Ｌの電位は上昇も下降もせず、位相オフセットが維持されたまま９０°位相検出回路１０１が動作し続けることになる。

【００６１】オフセットキャンセル回路３は、一層正確に９０°だけ位相を遅延させるために設けられている。オフセットキャンセル回路３において、抵抗Ｒ２はその一端に遅延調節信号Ｓ４を受け、他端はノードＣにおいてコンデンサＣＰ２の一端と差動アンプ３０の正入力端とが接続されている。コンデンサＣＰ２の他端は接地されている。差動アンプ３０の負入力端はノードＤにおいてトランジスタＭＰ２１，ＭＮ２０のドレインが共通して接続され、出力端はオフセットキャンセル信号Ｓ５を出力する。トランジスタＭＰ２１のソースには電源電位V_Dが与えられ、トランジスタＭＮ２０のソースは接地される。また、トランジスタＭＮ２０のゲートとドレインは共通に接続され、トランジスタＭＰ２１のゲートにはバイアス電位V_{BP}が与えられている。ここでトランジスタＭＰ２１，ＭＮ２０の特性はそれぞれトランジスタＭＰ１，ＭＮ１０と同一に揃えられており、トランジスタＭＰ２１，ＭＮ２０は、９０°位相検出回路１０１のトランジスタＭＰ１，ＭＮ１０のいわばダミーとして設

けられている。

【００６２】差動アンプ３０はノードＬの電位を間接的にノードＣにおいて受け、ノードＤの電位と比較する。ノードＤの電位はノードＫの電位と等しいと考えられるので、オフセットキャンセル信号Ｓ５はノードＫ，Ｌの電位差をキャンセルするように抵抗Ｒ３の値を調整することができる。

【００６３】ノードＬの電位は、ローパスフィルタ２と、抵抗Ｒ２，ＣＰ２とで構成されるローパスフィルタ２ｂとの２つのローパスフィルタを経由してノードＣへと伝達される。ローパスフィルタ２はコンデンサＣＰ１によりノードＬを流れる電荷の量を平均化し、それにより直流的な電圧信号である遅延調節信号Ｓ４を発生させる。この信号Ｓ４により遅延段５が制御された後、新たな平衡状態が生じそれに伴ってノードＬの電位もまた変化する。ここで、コンデンサＣＰ２の値をコンデンサＣＰ１の値よりも大きく設定するなどして、ローパスフィルタ２ｂの時定数をローパスフィルタ２の時定数よりも大きくすることで、ローパスフィルタ２ｂの出力であるノードＣの電位の変化を、ローパスフィルタ２の入力であるノードＬの電位の変化よりもゆっくりとしたものとすることができる。このような構成を採ることにより、一旦遅延が制御された後で、差動アンプ３０はゆっくりと抵抗Ｒ３の抵抗値の制御を行ない、平衡状態をほぼ維持しつつ、トランジスタＭＮ１２のゲート電位（つまりローパスフィルタ２の出力端の電位）がノードＤの電位と等しくなるようにすることができる。

【００６４】ちなみに、トランジスタＭＰ２１，ＭＮ２０はトランジスタＭＰ１，ＭＮ１０のダミーとして働くので、ノードＬからの信号が二つのローパスフィルタを通過してノードＣに至っていることと同様に、ノードＤにも二組のローパスフィルタが必要ではないかという懸念が生じるかもしれない。しかし平衡状態になったときにはノードＬからローパスフィルタ２へ流れ込む電流と流れ出す電流とは同じ値になるので、ローパスフィルタ２の機能によってトランジスタＭＮ１２のゲートには平均的にみて電流が流れない状態になっているといえる。つまりノードＣに接続されている抵抗Ｒ２にも、電流が流れることによる電圧降下は生じない。一方、ノードＤも差動アンプ３０という、入力インピーダンスの高い負入力端に接続されているため、電流は流れない。よってノードＤに対して二組のローパスフィルタを設ける必要はない。

【００６５】図１１は抵抗Ｒ３の構成を例示する回路図である。固定抵抗Ｒ４とＮｃｈトランジスタMN_{16}の直列接続によって抵抗Ｒ３が構成されている。トランジスタMN_{16}のゲート電位にオフセット補正信号Ｓ５を与えてトランジスタMN_{16}のＯＮ抵抗を変化させる。

【００６６】以上のように、本実施の形態ではノードＫ，Ｌの電位差を間接的にノードＣ，Ｄで検出し、その電位差に基づいてトランジスタＭＮ１２の流す電流を制御するフィードバックを行うので、ロック時においてノードＬの電位をノードＫの電位にほぼ一致させることができ、位相オフセットの問題を解決することができる。

【００６７】実施の形態４．図１２は本発明の実施の形態４にかかる９０°位相シフタのうち、図１８に示された９０°位相検出回路１００に置換して用いられる９０°位相検出回路１０３の構成を示す回路図である。９０°位相検出回路１０３は実施の形態１において示された９０°位相検出回路１０１における電流制御部１４を電流制御部１５に置換した構成を有している。

【００６８】電流制御部１５は電流制御部１４に対し、２つのＮｃｈトランジスタＭＮ１４，１５を追加した構成を備えている。具体的には、ノードＥにおいてトランジスタＭＮ１０のドレインとトランジスタＭＮ１４のソース及びバックゲートが、ノードＡにおいてトランジスタＭＰ１のドレインとトランジスタＭＮ１４のドレインとが、それぞれ接続されている。またノードＦにおいてトランジスタＭＮ１１のドレインとトランジスタＭＮ１５のソース及びバックゲートが、ノードＢにおいてＭＰ２のドレインとトランジスタＭＮ１５のドレインとが、それぞれ接続されている。ノードＥ，ＦにはＥＸＯＲ部１３が接続される。つまり、トランジスタＭＰ１，ＭＮ１４を一つの電流源として、またトランジスタＭＰ２，ＭＮ１５を他の一つの電流源として、それぞれ把握することができる。

【００６９】このような構成において、トランジスタＭＮ１４，ＭＮ１５のゲートに共通にバイアス電位V_{BN2}を与えることにより、以下のようにしてノードＥとノードＦの間の電位差を抑えることができる。

【００７０】ノードＡ、ノードＢ、ノードＥ、ノードＦの各電位をそれぞれＶａ、Ｖｂ、Ｖｅ、Ｖｆとする。図１２の回路が動作しているときは、ＥＸＯＲ部１３を構成している四本の直列接続体Ｎ１～Ｎ４のうちのどれか一本を介して常にグランドへ向かう電流が流れており、瞬間的にはノードＥとノードＦでの電流の値は異なっている。しかし平均的に見た場合、平衡状態にあればノードＥからもノードＦからもＥＸＯＲ部１３へ向けて流れる電流は同じ値になるといえる。またノードＢからローパスフィルタ２へ流れる電流も瞬間的には流入、流出のどちらかになっているのだが、平均的にはローパスフィルタ２へは電流は流れないことになる。

【００７１】するとトランジスタＭＮ１４，ＭＮ１５に流れる電流は平均して等しいことになる。この電流をI_0’とする。よって、数１、数２が成り立つ（例えばグレイ＆メイヤ著“アナログ集積回路設計技術（第二版）上”培風館、ｐ．６２参照）。

【００７２】

【数１】

$$Io' = \frac{k}{2}\frac{W}{L}(V_{BN2}-Ve-V_{TH})^2(1+\lambda(Va-Ve))$$

【００７３】【数２】

$$Io' = \frac{k}{2}\frac{W}{L}(V_{BN2}-Vf-V_{TH})^2(1+\lambda(Vb-Vf))$$

【００７４】但し、ｋはゲート容量と電荷の移動度の積、ＷとＬは各々トランジスタのゲート幅とゲート長、V_{TH}はトランジスタのしきい値電圧、λは短チャネル効果をそれぞれ示している。また、トランジスタＭＮ１４，ＭＮ１５のソースとバックゲート電位とが等しいので、トランジスタＭＮ１４とＭＮ１５の基板効果によるしきい値の差は無視している。

【００７５】$V_f=V_e+\delta V_{ef}$、$V_b=V_a+\delta V_{ab}$として数１、数２を書き換えて、

【００７６】【数３】

$$Io' = \frac{k}{2}\frac{W}{L}(V_{BN2}-Ve-V_{TH})^2(1+\lambda(Va-Ve))$$

【００７７】【数４】

$$Io' = \frac{k}{2}\frac{W}{L}(V_{BN2}-Ve-V_{TH}-\delta Vef)^2(1+\lambda(Va-Ve-\delta Vef+\delta Vab))$$

【００７８】を得る。更に数３と数４の差をとり、δV_{ab}とδV_{ef}の積または各々の二乗の項を無視することにより、以下の関係式が求められる。

【００７９】【数５】

$$\frac{\delta Vef}{\delta Vab}=\frac{\lambda(V_{BN2}-Ve-V_{TH})}{2(1+\lambda(Va-Ve))+\lambda(V_{BN2}-Ve-V_{TH})}$$

【００８０】上記文献によれば、λは通常０．０３～０．００５V^{-1}の値を持つことから、数５の値は１／１００以下の値となる。

【００８１】以上のことから、この９０°位相検出回路１０３が平衡状態に達し、ＵＰ／ＤＯＷＮ信号Ｓ３を出力するノードＢがそれとペアとなるノードＡの電位と異なっていても、カレントミラーを構成するトランジスタＭＮ１０、ＭＮ１１のドレイン部であるノードＥとノードＦの間には電位差はほとんどないようにできることがわかる。よって、両方のトランジスタを流れる電流を一致させることができ、９０°位相検出回路１０３のオフセットを抑制することができる。

【００８２】実施の形態５．図１３は本発明の実施の形態５にかかる９０°位相シフタのうち、図１８に示された９０°位相検出回路１００に置換して用いられる９０°位相検出回路１０４の構成を示す回路図である。９０°位相検出回路１０３は実施の形態４において示された９０°位相検出回路１０３における電流制御部１５を電流制御部１６に置換した構成を有している。

【００８３】電流制御部１６は電流制御部１５に対し、２つのＰｃｈトランジスタＭＰ９，ＭＰ１０を追加した構成を備えている。具体的には、ノードＧにおいてトランジスタＭＰ１のドレインとトランジスタＭＰ９のソース及びバックゲートが、ノードＡにおいてトランジスタＭＰ９のドレインとトランジスタＭＮ１４のドレインとが、それぞれ接続されている。またノードＨにおいてトランジスタＭＰ２のドレインとトランジスタＭＰ１０のソース及びバックゲートが、ノードＢにおいてＭＰ１０のドレインとトランジスタＭＮ１５のドレインとが、それぞれ接続されている。つまり、トランジスタＭＰ１，ＭＰ９，ＭＮ１４を一つの電流源として、またトランジスタＭＰ２，ＭＰ１０，ＭＮ１５を他の一つの電流源として、それぞれ把握することができる。

【００８４】このような構成において、トランジスタＭＰ９，ＭＰ１０のゲートに共通にバイアス電位V_{BP2}を与える。実施の形態４に示された電流制御部１５においては、ノードＡとノードＢの間に電位差があるときにトランジスタＭＰ１，ＭＰ２を流れる電流もドレイン電圧の違いにより若干差が生じることになる。しかし、本実施の形態では実施の形態４と同じ原理により、トランジスタＭＰ９、ＭＰ１０を挿入することで電流制御部１６のノードＧとノードＨの間の電位差を抑制することができるので、さらに高精度のオフセットキャンセル効果が実現できる。

【００８５】

【発明の効果】この発明のうち請求項１にかかる９０°位相シフタによれば、第１及び第２信号が異なる論理を採る時点では第１部分によって第１ノードから第２電流が引き抜かれるので、カレントミラー回路の第２経路には第１電流よりも第２電流の分だけ少ない電流が流れる。一方、第２電流源は第２ノードに第１電流を供給するので、第２電流が第２ノードから第１ローパスフィルタへと流出する。逆に第１及び第２信号が等しい論理を採る時点では第２部分によって第２ノードから第２電流が引き抜かれる。しかし、第１ノードからは電流が引き抜かれず、カレントミラー回路の第２経路には第１電流

が流れている。従って、第２電流が第２ノードへと第１ローパスフィルタから流入する。このような電流の流出入は第１ローパスフィルタにおいて積分され、遅延部の遅延量を制御する。遅延部では第１信号を遅延させて第２信号を生成するので、第１信号と第２信号とは９０°の位相差を保ってロックするようにフィードバック制御が行われる。

【００８６】この発明のうち請求項２にかかる９０°位相シフタによれば、第２ノードから第１ローパスフィルタに対して流出入する第２電流のジッタが、第１コンデンサと抵抗とで決定される時定数で抑制される。

【００８７】この発明のうち請求項３にかかる９０°位相シフタによれば、第１ローパスフィルタの出力電位を、初期状態において大きな値にすることにより、第２信号を得るための遅延値を小さくしてロックへの移行動作を行うことができる。

【００８８】この発明のうち請求項４にかかる９０°位相シフタによれば、ダミー部及び第１ローパスフィルタによって、それぞれ第１及び第２ノードの値をモニタすることができる。従って、第１及び第２ノードに電位差が生じて平衡状態に達しても、その差を抑制するように制御信号が遅延量を制御することができる。

【００８９】この発明のうち請求項５にかかる９０°位相シフタによれば、一旦遅延が制御された後で、差動増幅器がゆっくりと可変抵抗の抵抗値の制御を行なって、平衡状態をほぼ維持しつつ、位相シフトの抑制を行うことができる。

【００９０】この発明のうち請求項６にかかる９０°位相シフタによれば、第１電流源の第１トランジスタ及び第２電流源の第１トランジスタが、第１ノード及び第２ノードの電位差を小さくするので、カレントミラー回路の動作を確実にし、位相オフセットを抑制することができる。

【００９１】この発明のうち請求項７にかかる９０°位相シフタによれば、第１電流源の第３トランジスタ及び第２電流源の第３トランジスタが、更にカレントミラー回路の動作を確実にし、位相オフセットを一層抑制することができる。

【００９２】この発明のうち請求項８にかかるものによれば、出力ノードに第１電流源を接続するか否かを第１及び第２信号に基づいて第１スイッチが決定するが、第１スイッチに対して第１及び第２信号の負荷は等しい。また、出力ノードに第２電流源を接続するか否かを第１及び第２信号に基づいて第２スイッチが決定するが、第２スイッチに対しても第１及び第２信号の負荷は等しい。従って、第１及び第２信号についての負荷を均等にして、位相オフセットを抑制することができる。

【図面の簡単な説明】

【図１】　本発明の実施の形態１の構成を示す回路図である。

【図２】　本発明の実施の形態１の動作を示す回路図である。

【図３】　本発明の実施の形態１の動作を示す回路図である。

【図４】　本発明の実施の形態１の動作を示すタイミングチャートである。

【図５】　本発明の実施の形態１の構成を示す回路図である。

【図６】　本発明の実施の形態１の構成を示す回路図である。

【図７】　本発明の実施の形態１の動作を示すタイミングチャートである。

【図８】　本発明の実施の形態１の動作を示すタイミングチャートである。

【図９】　本発明の実施の形態２の構成を示す回路図である。

【図１０】　本発明の実施の形態３の構成を示す回路図である。

【図１１】　本発明の実施の形態３の構成を示す回路図である。

【図１２】　本発明の実施の形態４の構成を示す回路図である。

【図１３】　本発明の実施の形態５の構成を示す回路図である。

【図１４】　従来の技術を示すタイミングチャートである。

【図１５】　従来の技術を示すタイミングチャートである。

【図１６】　従来の技術を示す回路図である。

【図１７】　従来の技術を示す回路図である。

【図１８】　従来の技術を示す回路図である。

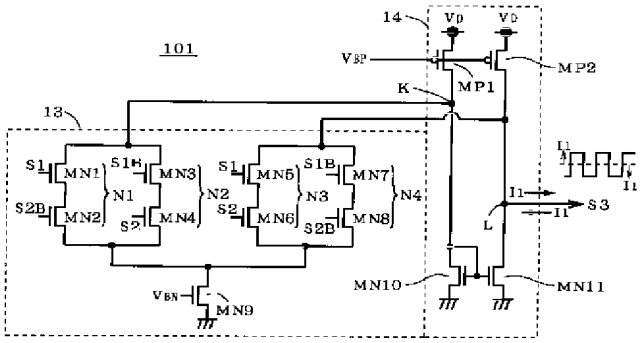
【図１９】　従来の技術を示す回路図である。

【図２０】　従来の技術を示す回路図である。

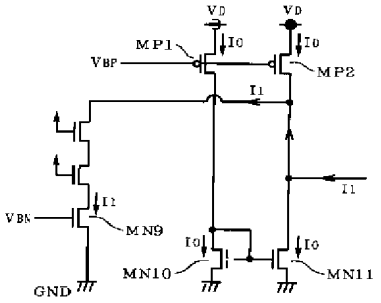
【符号の説明】

Ａ，Ｂ，Ｅ，Ｆ，Ｇ，Ｈ，Ｋ，Ｌ，Ｗ　ノード、I_1，I_0，I_0’　電流、２，２ｂ　ローパスフィルタ、１３，１３ａ，１３ｂ　ＥＸＯＲ部、１４～１６，１４ａ，１４ｂ　電流制御部、５　遅延段、３０　差動増幅器、５０　遅延調節回路、５１　遅延バッファ部、Ｓ１，Ｓ２　クロック、Ｓ３　ＵＰ／ＤＯＷＮ信号、Ｓ４　遅延調節信号、Ｒ１～Ｒ３　抵抗、ＣＰ０～ＣＰ２　コンデンサ、ＳＷ　スイッチ、Ｄ１　ダイオード、V_{BN}，V_{BN2}，V_{BP}，V_{BP2}　バイアス電位。

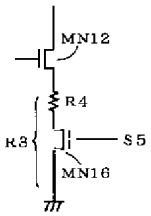
【図1】



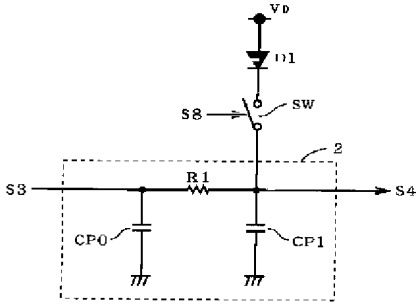
【図2】



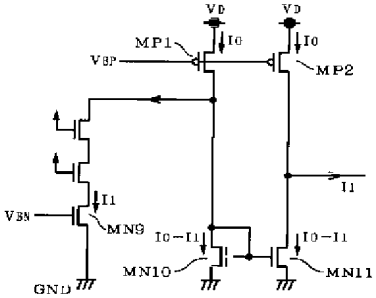
【図11】



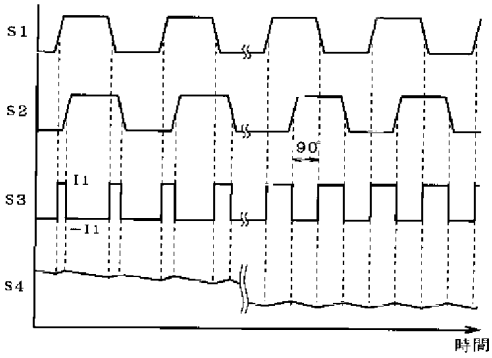
【図6】



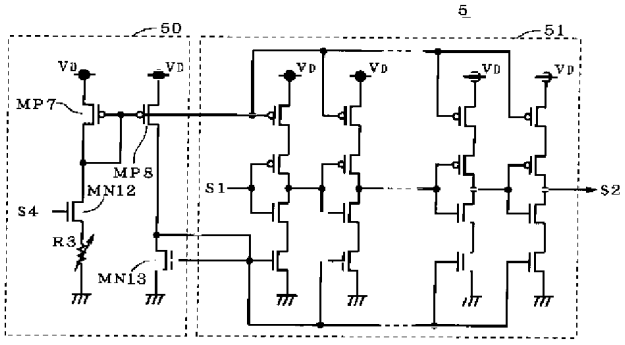
【図3】



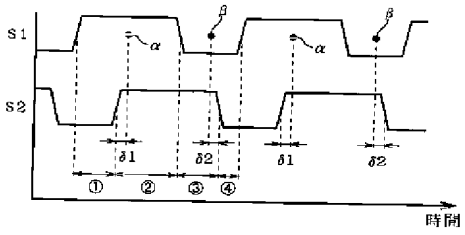
【図4】



【図5】



【図7】



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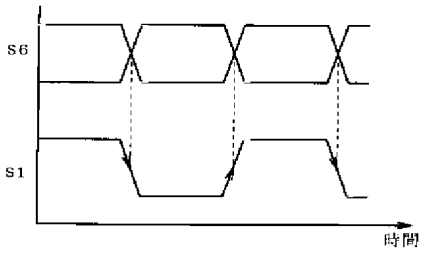

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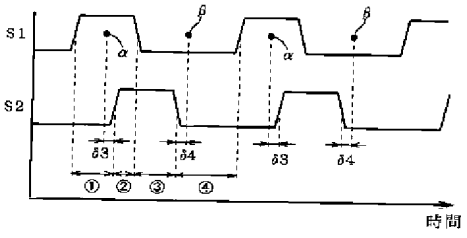

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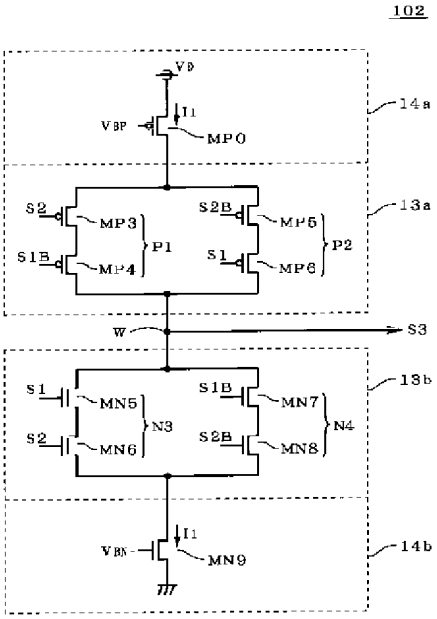

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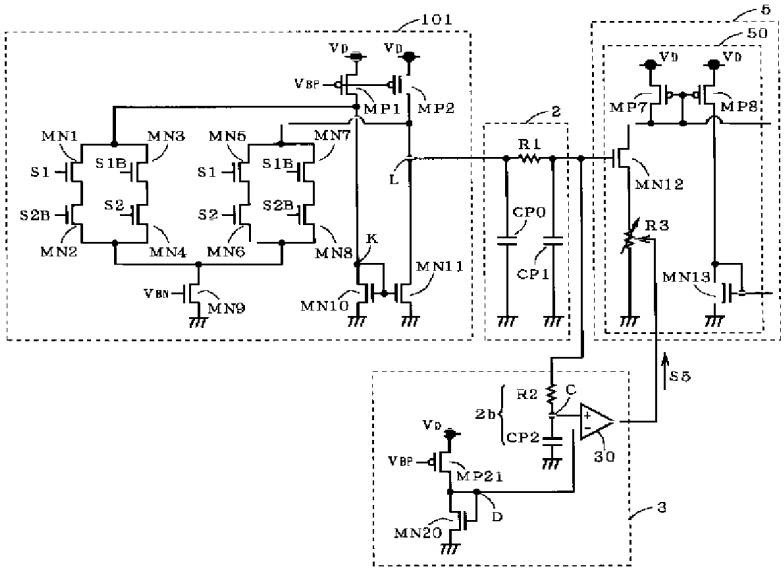

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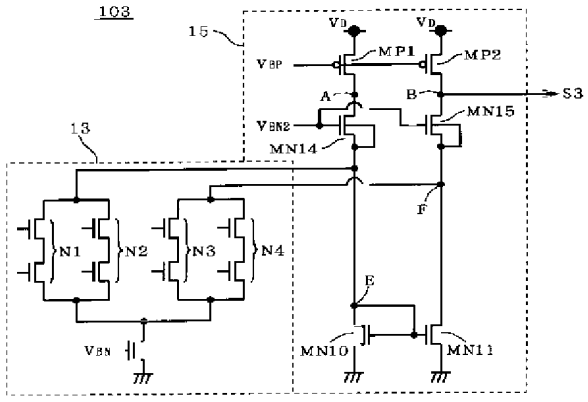

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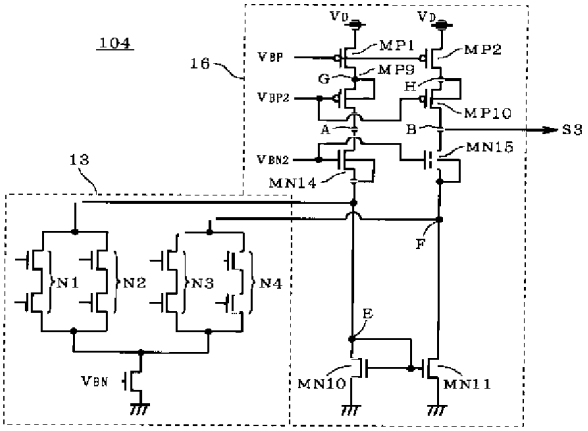

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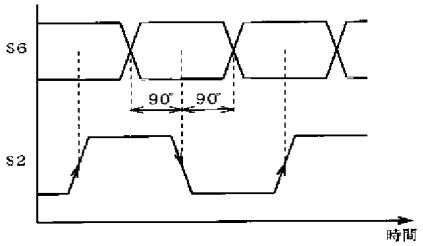

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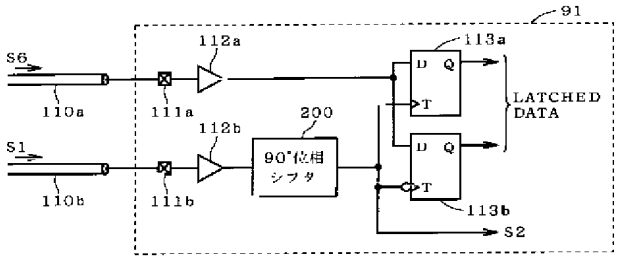

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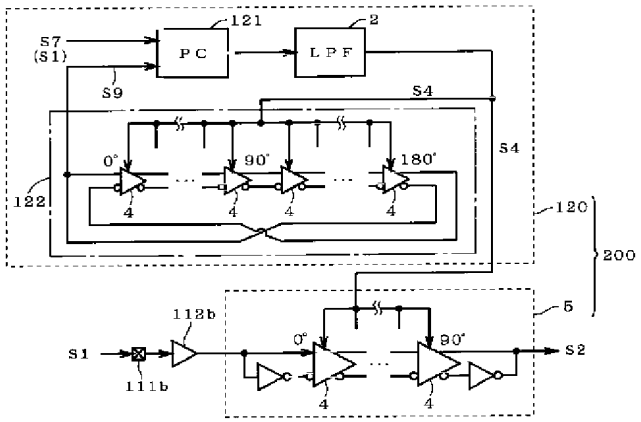

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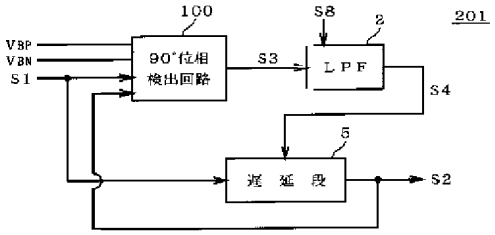

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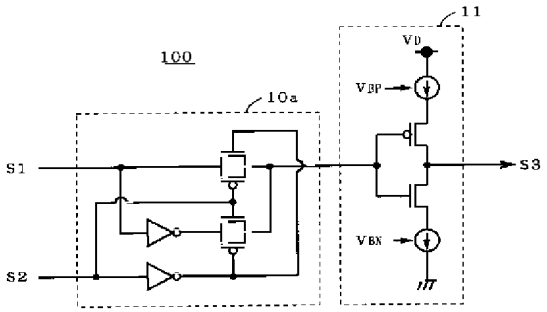

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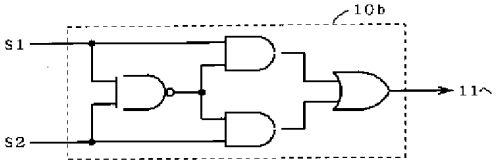

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